**ISTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY**

# A NEW CONTROL METHOD FOR MULTI-OUTPUT FORWARD CONVERTERS

**M.Sc. Thesis by**

**Şükrü ERTİKE, B.Sc.**

**Department : Electrical Engineering**

**Programme: Electrical Engineering**

**Supervisor : Assist. Prof. Dr. Deniz YILDIRIM**

**JANUARY 2007**

**ISTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY**

# A NEW CONTROL METHOD FOR MULTI-OUTPUT FORWARD CONVERTERS

**M.Sc. Thesis by**

**Şükrü ERTİKE, B.Sc.**

**(504031044)**

**Date of submission : 25 December 2006**

**Date of defence examination : 29 January 2007**

**Supervisor (Chairman) : Assist. Prof. Dr. Deniz YILDIRIM**

**Members of the Examining Committee : Assist. Prof. Dr. Özgür ÜSTÜN**

**Assist. Prof. Dr. Metin AYDIN (KU)**

**JANUARY 2007**

**İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ**

# ÇOK ÇIKIŞLI FORWARD ÇEVİRİCİLER İÇİN YENİ BİR KONTROL YÖNTEMİ

**YÜKSEK LİSANS TEZİ**

**Müh. Şükrü ERTİKE**

**(504031044)**

**Tezin Enstitüye Verildiği Tarih : 25 Aralık 2006**

**Tezin Savunulduğu Tarih : 29 Ocak 2007**

**Tez Danışmanı : Yrd.Doç.Dr. Deniz YILDIRIM**

**Diğer Jüri Üyeleri : Yrd.Doç.Dr. Özgür ÜSTÜN**

**Yrd.Doç.Dr. Metin AYDIN (KÜ)**

**OCAK 2007**

**ACKNOWLEDGEMENTS**

It was a very nice and thoughtful experience to work with my supervisor Asist. Prof. Deniz YILDIRIM. Thanks to him for contribution of this study.

Thank you my friends; Selin PARLAR, Filiz GÜRGÖZE, Alper ONUR and my other colleagues at ITU Electrical Machines Laboratory for their encouragement and support through my study.

I am grateful to my lovely family; I thank you for everything that you have done for me so far.

**December 2006** **Şükrü ERTİKE**

**INDEX**


**ACKNOWLEDGEMENTS** iii
**INDEX** iv
**ABBREVIATIONS** vi
**LIST OF TABLES** vii
**LIST OF FIGURES** viii
**LIST OF SYMBOLS** x
**SUMMARY** xi
**ÖZET** xii

**1. INTRODUCTION** 1
**1.1. Problem Definition** 1

**2. MULTI OUTPUT FORWARD CONVERTERS in LITERATURE** 3
**2.1. Use of Magamps As Post Regulators** 3
**2.2. Weighted Voltage Mode Control** 3
**2.3. Parallel Regulation Method** 4
**2.4 Synchronous Switch Post Regulator** 5
**2.5. Time Shared Controlled Current Source Based Converter** 5
**2.6. Voltage Feed Forward Synchronous Forward Converter** 6
**2.7. Voltage Feed Forward Synchronous Forward Converter with Automatic Master Slave Assignment** 7

**3. A NEW CONTROL SCHEME and TOPOLOGY for MULTI-OUTPUT FORWARD CONVERTERS** 8
**3.1. Description and Operation of Proposed MOFC** 8
**3.2. Averaged Switch Modeling of Proposed Converter** 10
**3.2.1. Large Signal Model for CCM Case** 12
**3.2.2. Small Signal Model for CCM Case** 13
**3.2.3. Transfer Functions for CCM Case** 16
**3.2.3.1. Line to Output Transfer Function** 16
**3.2.3.2 Control to Output Transfer Function** 17
**3.2.3.3. Output Impedance in CCM** 18
**3.2.4. Large Signal Model for DCM Case** 18
**3.2.5. Small Signal Model for DCM Case** 20
**3.2.6. Transfer Functions for DCM Case** 21
**3.2.6.1. Line to Output Transfer Function** 22
**3.2.6.2 Control to Output Transfer Function** 22
**3.2.6.3. Output Impedance in DCM** 23

**4. SIMULATION RESULTS** **24**
**4.1. Line Regulation of the MOFC with Proposed Concept** **25**
**4.1.1 Some Key Waveforms of the Two-Output Forward Converter with Proposed Control Concept** **26**
**4.2. Load Regulation of the MOFC with Proposed Concept** **30**
**4.3. Load Regulation of the Two-Output Forward Converter with Conventional Master Slave Based Control** **35**

**5. CONCLUSION and FUTURE WORKS** **40**

**REFERENCES** **43**

**APPENDIX A** **45**

**APPENDIX B** **47**

**BIOGRAPHY** **51**

**ABBREVIATIONS**

| | |
|---|---|
| **SMPS** | : Switch Mode Power Supply |
| **MOFC** | : Multi Output Forward Converter |
| **WVMC** | : Weighted Voltage Mode Control |
| **CCM** | : Continuous Conduction Mode |
| **DCM** | : Discontinuous Conduction Mode |
| **SSPR** | : Synchronous Switch Post Regulator |

## LIST OF TABLES


| | | Page Number |
|---|---|---|
| **Table 3.1** | Small signal parameters of MOFC for DCM case…….. | 21 |
| **Table 5.1** | Comparison of proposed converters in the literature……. | 46 |

## LIST OF FIGURES

**Page Number**


**Figure 1.1** : PUPS and Multi-Output Power Supply……..... ……1
**Figure 1.2** : Conventional master-slave based multi-output forward converter..... ……2
**Figure 2.1** : A two output forward converter with a Magamp..... ……3
**Figure 2.2** : A Multi-Output Forward Converter with WVMC..... …….4
**Figure 2.3** : Two output forward converters controlled with parallel regulation method…… ……4
**Figure 2.4** : Two-output forward converter with SSPR..... ……5
**Figure 2.5** : Two output buck converter with a time shared controlled current source…….. …….6
**Figure 2.6** : Multi-output forward converter with voltage feed forward control and SSPR……. …….6
**Figure 2.7** : Multi-output forward converter wit automatic master slave control…….. ……7
**Figure 3.1** : Multi-output forward converter with proposed control scheme …….8
**Figure 3.2** : Structure of output controllers at proposed MOFC…… ……9
**Figure 3.3** : Structure of main witch controller……. 10
**Figure 3.4** : Defined switch network in the proposed MOFC (left) and equivalent averaged circuit (right) for CCM case…….. ……..11
**Figure 3.5** : Defined switch network in the proposed MOFC (left) and equivalent averaged circuit (right) for DCM case…….. .....…11
**Figure 3.6** : Key waveforms of the multi-output forward converter for CCM case…… ……...12
**Figure 3.7** : Large signal equivalent circuit of proposed n-output forward converter for CCM case……. ……..13
**Figure 3.8** : Small signal equivalent circuit of proposed n-output forward converter for CCM case……. ……..16
**Figure 3.9** : Key waveforms of the multi-output forward converter for DCM case……..……. ……..19
**Figure 3.10** : Large signal equivalent circuit of proposed n-output forward converter for DCM case…….. ……..21
**Figure 4.1** : Two-output forward converter which is simulated with proposed control scheme…… …….25
**Figure 4.2** : Two-output forward converter for line regulation test…….. …….26
**Figure 4.3** : Change of input voltage during line regulation test……. ……..26
**Figure 4.4** : Regulations of output voltages against line variations…… ……..27
**Figure 4.5** : Main switch current and voltage waveforms…….. ……..28
**Figure 4.6** : Switch network output current and voltage waveforms for 5V-output…….. ……..29

**Figure 4.7 :** Switch network output current and voltage waveforms for 12V-output…….. ……..30
**Figure 4.8 :** Gating signals of the output switches……. ……30
**Figure 4.9 :** Gating signals of the main switch……... ……..31
**Figure 4.10 :** Two-output forward converter for load regulation test…….. ……..31
**Figure 4.11 :** Variations of output currents during load regulation tests……. ……..32
**Figure 4.12 :** Load regulation of the output voltages under proposed control method…… ……..32
**Figure 4.13 :** Close view of the 5V-output voltage waveform during load regulation…… ……..33
**Figure 4.14 :** Close view of the 12V-output voltage waveform during load regulation test……. ……..33
**Figure 4.15 :** Two-output forward converter for load regulation test (from no-load to full-load variation case)…… ……..34
**Figure 4.16 :** Variations of output currents during load regulation tests (from no-load to full-load)……. ……..34
**Figure 4.17 :** Close view of the 5V-output voltage waveform during load regulation test (from no-load to full-load)……... ……..35
**Figure 4.18 :** Close view of the 12V-output voltage waveform during load regulation test (from no-load to full-load)……. ……35
**Figure 4.19 :** Two-output forward converter with master-slave based control method……. ……..36
**Figure 4.20 :** Variation of 5V (red) and 12V-output (blue) currents in master-slave based forward converter……. ……..37
**Figure 4.21 :** Variation of 5V (red) and 12V-output (blue) voltages in master-slave based forward converter……. ……37
**Figure 4.22 :** Variation of 5V (red) and 12V-output (blue) currents in master-slave based forward converter; master-output goes from full-load to no-load……. ……37
**Figure 4.23 :** Variation of 5V (red) and 12V-output (blue) voltages in master-slave based forward converter; master-output goes from full-load to no-load……. ……..38
**Figure 4.24 :** Variation of 5V (red) and 12V-output (blue) currents in master-slave based forward converter; slave-output goes from full-load to no-load…….. ……..39
**Figure 4.25 :** Variation of 5V (red) and 12V-output (blue) voltages in master-slave based forward converter; slave-output goes from full-load to no-load……. ……40

## TABLE OF SYMBOLS

$V_g$ : Input dc voltage source

$v_g$ : Instantaneous value of input dc voltage source

$i_{Lm}$ : Instantaneous value of magnetizing current

$i_{S_m}$ : Instantaneous value of main switch (mosfet) current

$v_{S_m}$ : Instantaneous value of main switch (mosfet) voltage

$i_{S_{ok}}$ : Instantaneous value of the k$^{th}$ output inductance current

$v_{S_{ok}}$ : Instantaneous value of the output voltage of k$^{th}$ switch network

$n_k$ : Turn ratio between primary winding and k$^{th}$ output winding

$n_r$ : Turn ratio between primary winding and reset winding

$L_m$ : Magnetizing inductance

$L_{ok}$ : Output inductance of the k$^{th}$ output

$C_{ok}$ : Filter capacitor of the k$^{th}$ output

$R_{ok}$ : Load resistor of the k$^{th}$ output

$D_k$ : Duty cycle of the k$^{th}$ output at steady state

$d_k$ : Instantaneous duty cycle of the k$^{th}$ output

$d_{k1}$ : Duty cycle of the k$^{th}$ output in DCM

$d_{k2}$ : Conduction duty of the k$^{th}$ output in DCM

$d_{k3}$ : No-conduction duty of the switches at k$^{th}$ output in DCM

$v_c$ : Common sawtooth carrier voltage

$v_{ref_k}$ : Reference voltage of the k$^{th}$ output

$\langle x \rangle$ : Average value of $x$ over one switching period

$\hat{x}$ : Small signal representation of $x$

$Z_{ki}$ : Output impedance corresponding to $i$th output.

## A NEW CONTROL METHOD FOR MULTI OUTPUT FORWARD CONVERTERS


## SUMMARY

Forward type switch mode power supplies (SMPS) are widely used in industry for variety of purposes such as computer power supplies, automotive and industrial electronics applications. There is a great interest on the design of SMPSs to reduce cost, minimize space requirement and improve quality. Especially, designing isolated multiple-output power supplies provides a dramatic economy and constitutes a minimal space requirement. However, multiple output designs have inherent drawbacks with respect to performance of power supply. Main problems arising from such designs are: 1) because output windings are wound on the same magnetic core, there is electromagnetic coupling between different outputs, namely "cross regulation", 2) the possibility of varying operation mode (continuous or discontinuous current mode) of one or more output as a result of load variations. These two problems make design of multi-output SMPS difficult to constitute precisely and independently regulated output voltages. The solution or minimization of the first problem is the topic of transformer or more generally magnetic design of SMPS. On the other hand, second problem is subjected to control design because SMPS's transfer functions greatly changes with the operation mode. Cost effective solutions of those problems are still being investigated.

In this work a new control scheme and topology is proposed for precise and independent regulation of each output in multi-output forward converters with wide load variations. High performance operation of proposed converter is independent of continuous or discontinuous conduction mode operation of any output. Proposed method is developed for an n-output forward converter and is modeled for both continuous and discontinuous conduction of operation. Developed method is applied to a two-output forward converter and is verified by simulations.

## ÇOK ÇIKIŞLI FORWARD ÇEVİRİCİLER İÇİN YENİ BİR KONTROL YÖNTEMİ


## ÖZET

Forward türü anahtarlamalı güç kaynakları (AGK), endüstride kendisine oldukça geniş bir uygulama alanı bulmaktadır, kullanım alanlarına örnek olarak bilgisayar güç kaynakları, otomotiv ve endüstriyel elektronik uygulamaları verilebilir. AGK'ların düşük maliyetle, az yer kaplayacak şekilde ve yüksek performans kriterleriyle tasarımına yönelik büyük bir ilgi bulunmaktadır. Özellikle, izoleli çok çıkışlı AGK'lar küçük boyut ve düşük maliyet unsurlarını barındırdıklarından ayrı bir ilgi konusudurlar. Bununla birlikte çok çıkışlı AGK'ların performans açısından yapısal etkenlere ve yüklenme koşullarına bağlı olarak bazı dezavantajları vardır. Çok çıkışlı AGK tasarımında karşılaşılan temel sorunlar: 1) çıkış sargılarının aynı manyetik nüveyi paylaşmalarından dolayı, farklı çıkışların arasında manyetik bir bağ bulunması bir çıkışın yükündeki değişimin diğer çıkış gerilimlerini etkilemesi, literatürdeki ismiyle "çapraz regülasyon" problemi, 2) yüklenme durumuna bağlı olarak kimi çıkışların sürekli akım kipinde çalışırken kimi çıkışların süreksiz akım kipinde çalışması durumudur. Bu iki problem çok çıkışlı AGK'ların tasarımını zorlaştıran ve yüksek performans elde edilmesini engelleyen etkenlerdir. Çapraz regülasyon sorunu, transformatör ya da daha genel bir ifadeyle manyetik tasarım kısmına ait bir inceleme konusudur ve iyileştirilmesi büyük ölçüde manyetik tasarıma bağlıdır. İkinci problem ise kontrolör tasarımına ait bir konudur çünkü AGK'ların transfer fonksiyonu çalışma kipinin değişmesiyle birlikte değişim göstermektedir ve bu durum geniş bir yük aralığında çok çıkışlı AGK'ların yüksek performansla kontrol edilebilmesini oldukça zorlaştırmaktadır. Endüstride ve literatürde belirtilen problemlerin düşük maliyetle çözümüne yönelik araştırmalar devam etmektedir.

Bu çalışmada, çok çıkışlı forward türü anahtarlamalı güç kaynakları için her bir çıkışın geniş bir yük aralığında birbirinden bağımsız olarak ve çok hassas bir şekilde regüle edilebildiği yeni bir kontrol yöntemi ve topoloji önerilmektedir. Önerilen çeviricinin yüksek performansta çalışması çıkışların sürekli ya da süreksiz akım kipinde bulunmalarından bağımsızdır. Önerilen yöntem n sayıda çıkışı olan bir forward çevirici için geliştirilmiştir. Çevirici n-çıkışlı olarak sürekli ve süreksiz akım kipinde çalışma durumları için modellenmiştir. Geliştirilen yöntem iki çıkışlı bir forward çeviriciye uygulanmış ve benzetim yolu ile doğrulanmıştır.

## 1. INTRODUCTION

This work proposes a new control method and topology for multi output forward converters. Proposed converter is modeled in detail and new control concept is verified by simulations.

### 1.2 PROBLEM DEFINITION

Forward converters are widely used in industry for variety of purposes such as computer power supplies, automotive and telecom applications. In case of a multi-load application, using one converter with multiple outputs rather than a point-of-use power supplies (PUPS) for each load greatly reduces cost and minimizes space requirement. In this respect, forward converters are good candidates for multi-load applications. Figure 1.1 shows the usage of PUPS and a multi-output power supply for a multi-load application.

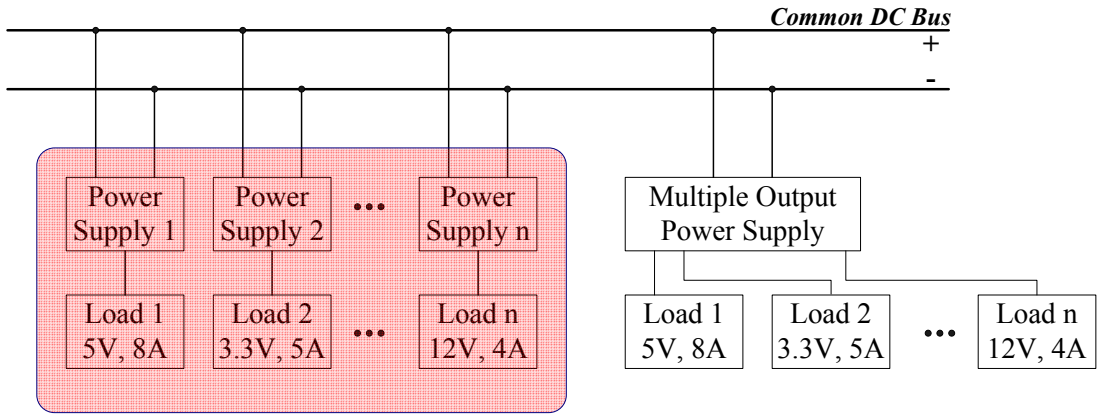


**Figure 1.1** PUPS and Multi-Output Power Supply

However, independent and precise voltage regulation of each output for operation with wide load ranges becomes a design problem for forward converters because of the cross-coupling effect between different outputs. Any load change in one output affects the voltages of other outputs. In applications where the loads are changing in wide ranges, conventional master-slave based control is not sufficient.

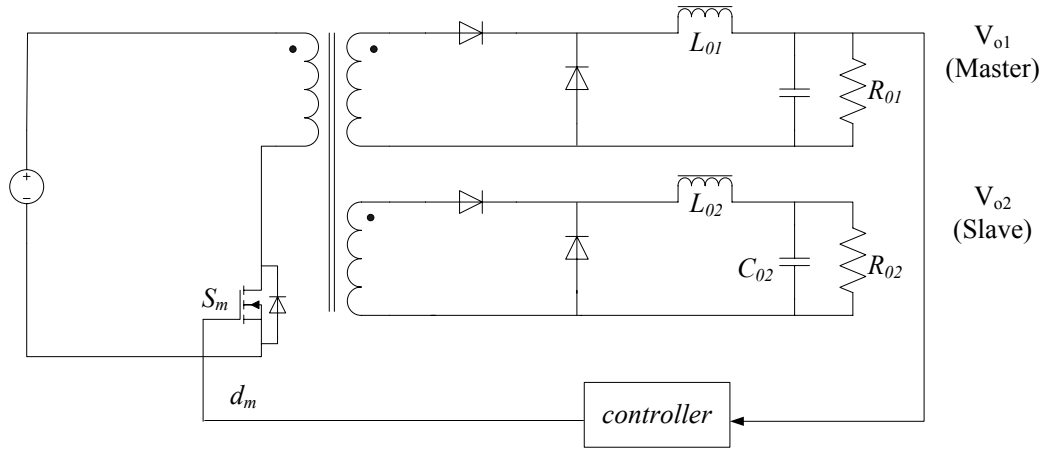


**Figure 1.2:** Conventional master-slave based multi-output forward converter.

As seen from Figure1.2, there is only one control loop and feedback parameter which are the duty cycle of main switch and the main output voltage respectively. Slave outputs try to follow the voltage of main output during operation. Regulation of the any slave output voltage depends highly on the operation mode of main output and the turns ratio of the transformer. For example, if the main output operates at no load while slave outputs operates at their rated (full) loads, controller will reduce duty cycle of main switch and the slave outputs will experience lack of power and will loose their regulations such that all slave output voltages decrease nearly to zero. On the other hand, while the main output operates at full load if any of the slave output operates at no load, in this case controller will increase duty cycle of the main switch to its maximum value and the slave output voltage will increase and loose regulation. Thus, only the main output can be regulated precisely in a master-slave based multi-output forward converter.

In multi load applications that require precise and independent regulation for each load voltage conventional master-slave based control can not be used. Using multi-output forward converters for such applications necessarily requires some modifications in control and topological arrangements. Existing solutions to the problem of designing multi-output forward converters are either very complicated and costly or do not have enough performance with respect to voltage regulation. This work is an investigation and proposal of a novel MOFC topology having the properties of simplicity and high performance regulation capability of each output.

## 2. MULTI-OUTPUT FORWARD CONVERTERS in LITERATURE

### 2.1 Use of Magamps as Post Regulators [1-6]

Magamp is a saturable reactor is used at one or more output as an additional switch. Figure 2.1 shows a MOFC with a Magamp at its one output as a post regulator. This method requires an extra resetting circuit for each Magamp and is a master-slave based solution. Main switch duty cycle must be higher than that of slave output, otherwise regulation is lost at the slave output. Implementation difficulty is reported as a common drawback of this method.

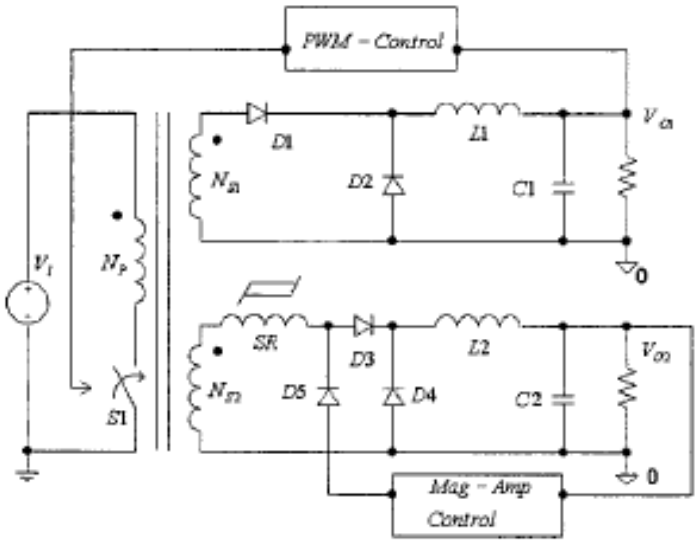


**Figure 2.1:** A two output forward converter with a Magamp [3].

### 2.2 Weighted Voltage Mode Control (WVMC) [7-9]

In this method, two or more outputs are sensed simultaneously and the weighted sums of all output voltages are fed back. None of the outputs can be regulated precisely; there is always a steady-state error at each output. Error is distributed amongst the outputs. This scheme is not suitable for applications where loads are changing in wide load ranges. Figure 2.2 shows the concept of WVMC for multi-output forward converters. This method is used widely in practice where regulation specifications are not so tight for slave outputs of a MOFC.

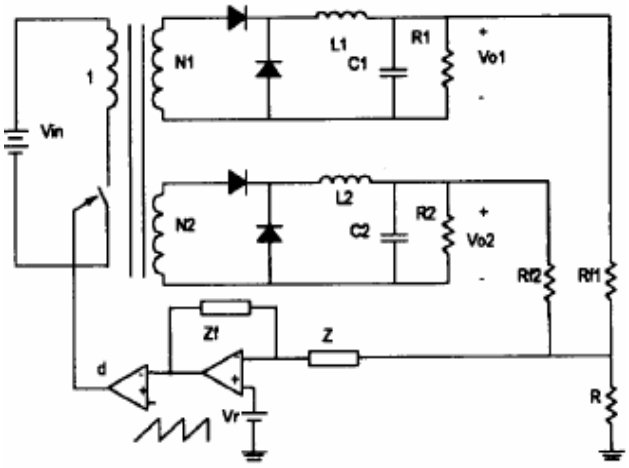


**Figure 2.2:** A Multi-Output Forward Converter with WVMC [7].

## 2.3 Parallel Regulation Method [10]

This method requires an additional boost converter for the regulation of each auxiliary output as illustrated in Figure 2.3. Application is limited to loads where the main output duty cycle variation is ±25%. This method greatly eliminates cross coupling between outputs. Design guideline is not reported for more than two-output case. Although regulation performance of this method is good, it becomes complicated as the number of outputs increases. It is a high cost solution because of the auxiliary converter(s).

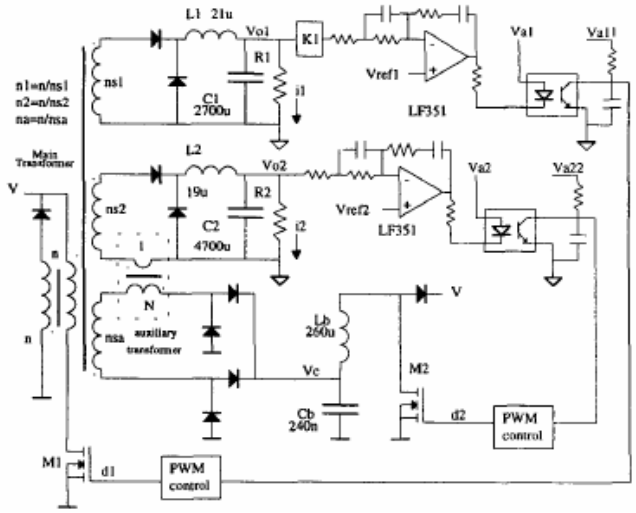


**Figure 2.3:** Two-output forward converter controlled by parallel regulation method.

## 2.4 Synchronous Switch Post Regulator (SSPR) [11]

This scheme given in Figure 2.4 for a two-output forward converter is conceptually very similar to forward converter with Magamp post regulation. The regulation of auxiliary output depends on the loading rate of the main output. If the main output works at light load, auxiliary output may experience lack of power and loose output voltage regulation.

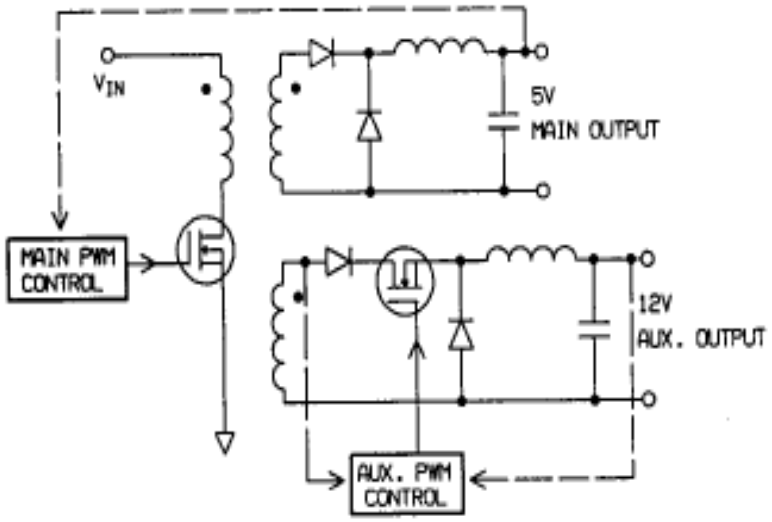


**Figure 2.4:** Two-output forward converter with SSPR [11].

## 2.5 Time-Shared-Controlled Current Source Based Converter [12]

Although this method is not directly applicable to multi-output forward converters, it is a very successful solution for non-isolated multi-load applications. In this method, a current source (input) is connected to each output for a specified time interval, i.e, loads share the current source in time. Application to forward converters is possible but control and power circuit may become more complex than that of multi-output buck converter. Operating frequencies of output switches are much lower than that of the switch at the input. Figure 2.5 shows a multi-output buck converter application of this method.

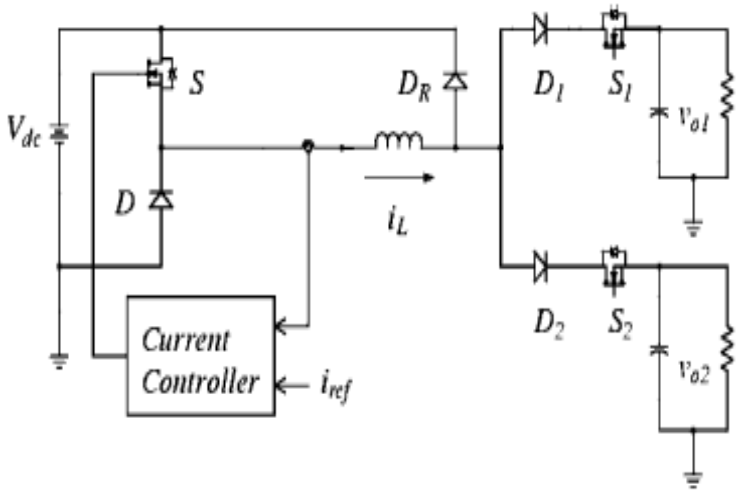


**Figure 2.5:** Two-output buck converter with a time shared controlled current source [12].

## 2.6 Voltage Feed Forward Synchronous Forward Converter [13, 14]

Cross coupling between outputs is removed by post regulators (controllers). This up-to-date solution provides regulation for wide load ranges. Topology and control method requires short circuiting of output synchronous rectifiers $SR_{k1}$ and $SR_{k2}$, therefore additional current limiting inductances are necessary for each output. Here $k$ represents the $k^{th}$ output, $k=1,2,...,n$. Primary switch duty cycle is always kept nearly constant independent from outputs. Regulation of the $k^{th}$ output is constituted by adjusting the duty cycle of freewheeling MOSFET $SR_{k2}$. It is a very successful solution in terms of regulation performance and simplicity of topology. Figure 2.6 shows a two output forward converter application of this method.

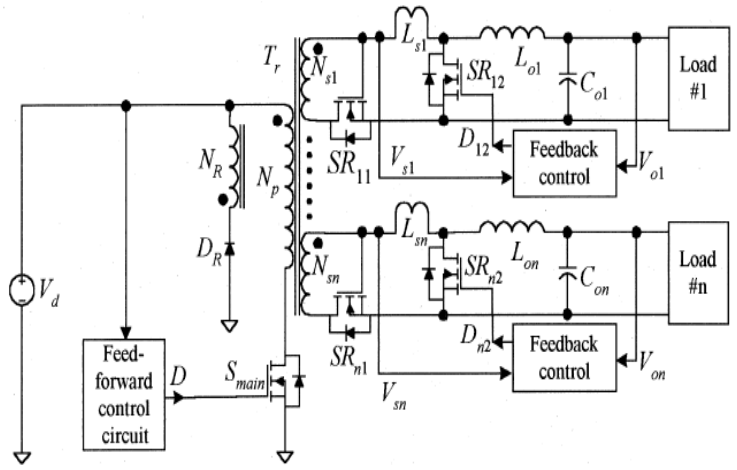


**Figure 2.6:** Multi-output forward converter with voltage feed forward control and SSPR [13]

## 2.7 Voltage Feed Forward Synchronous Forward Converter with Automatic Master Slave Assignment [15]

This method is an improved version of the work given in section 2.6. Primary and secondary controllers are coupled to obtain automatic master-slave selection. Automatic master-slave logic circuit is complicated and concept is verified by simulation. Figure 2.7 shows the application of the method to a two-output forward converter.

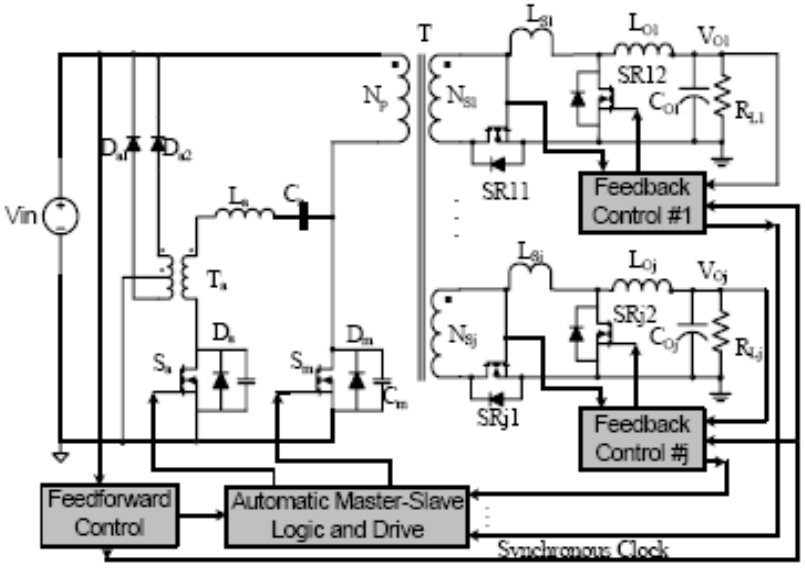


**Figure 2.7:** Multi-output forward converter with automatic master-slave control.

## 3. A NEW CONTROL SCHEME and TOPOLOGY for MULTI-OUTPUT FORWARD CONVERTERS

In this section, a new control scheme and topology for MOFCs (multi-output forward converter) is proposed. After giving the description and operation of the proposed concept, detailed mathematical modeling of the n-output forward converter for continuous conduction mode (CCM) and discontinuous conduction mode (DCM) cases are derived based on averaged switch modeling technique given in [16].

### 3.1 Description and Operation of Proposed MOFC

Figure 3.1 shows the proposed multi-output forward converter topology. Each output has a controlled switch $S_k$, $k=1, 2, \ldots n$, on the forward path differing from a conventional forward converter that utilizes only one controlled switch at the primary.

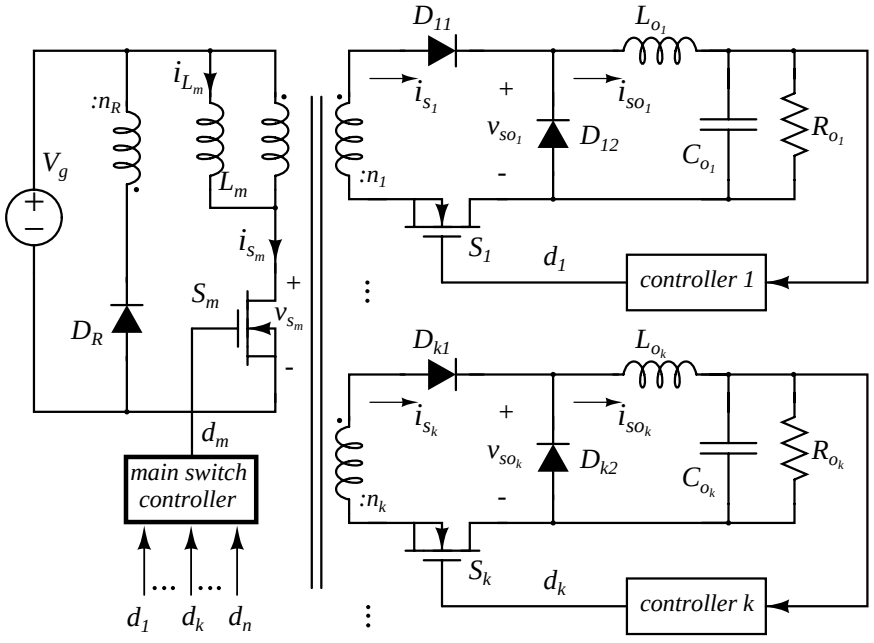


**Figure 3.1:** Multi-output forward converter with proposed control scheme.

With this modification each output becomes a widely known buck converter with an additional diode $D_{k1}$ in series with switch $S_k$. Transformer flux balance is achieved by

a reset winding having the same number of turns with the primary winding. In order to reduce switching losses and increase duty cycle limit of the primary switch $S_m$, soft switching and active clamp techniques can be employed. The diode $D_{k1}$ is used to prevent the reversal of current direction during DCM operation and transient cases. The freewheeling diode $D_{k2}$ can be replaced with a MOSFET for synchronous rectification enabling further loss reduction for high current applications. As shown in Figure 3.2, there is a dedicated controller for each output performing the necessary voltage mode control and produces duty cycle $d_k$ for switch $S_k$. Duty cycle $d_k$ is produced by comparing the $k^{th}$ output error signal with a common saw-tooth carrier.

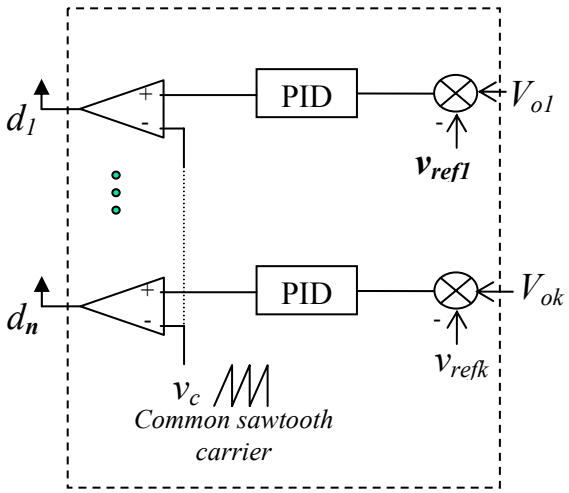


**Figure 3.2:** Structure of output controllers at proposed MOFC

Duty cycle of primary switch $S_m$ is extracted from the calculated duty cycles of each output. The control law for $d_m$ is very simple:

$$d_m = \max\left(d_1, d_2, .., d_k ..., d_n\right) \tag{3.1}$$

With this control scheme, the duty cycle of $S_m$ will be the same as that of output requiring the greatest duty cycle and the duty cycles of all other outputs will be lower than $d_m$. This scheme not only constitutes an automatic master-slave assignment but also guarantees that none of the outputs experiences lack of power/voltage regulation at any loading conditions. In addition, since the primary switch duty cycle is adjusted according to load and line variations (indirectly), this arrangement also reduces transformer losses, keeping the magnetizing current of the transformer just as much

as necessary for the load condition. The main switch controller realizing the equation (3.1) is just an OR operation and shown in Figure 3.3.

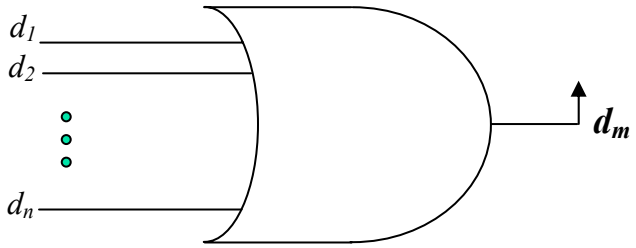


**Figure 3.3:** Structure of main switch controller.

In summary, the operation of the proposed MOFC is very similar to conventional forward converter except that each output power stage has different duty cycles decoupled from others. Key waveforms of the converter will be given in the following section.

### 3.2 Averaged Switch Modeling of Proposed Converter

In this section, averaged switch model of the proposed multi-output forward converter is derived. Large and small signal equivalent circuits and converter transfer functions are also given.

Averaged switch modeling technique described in [16] is very useful to model dc-dc converters for both CCM and DCM. In this method a switch network is defined in the converter. Then, the electrical quantities corresponding to input and output ports of the switch network are averaged over one switching period. Finally, the actual switch network is replaced by the equivalent time-invariant circuit with respect to circuit connections representing the averaged port quantities of the switch network. That approach greatly simplifies the analysis of the converter system because averaged switch network consists of dependent voltage/current or power sources rather than switches.

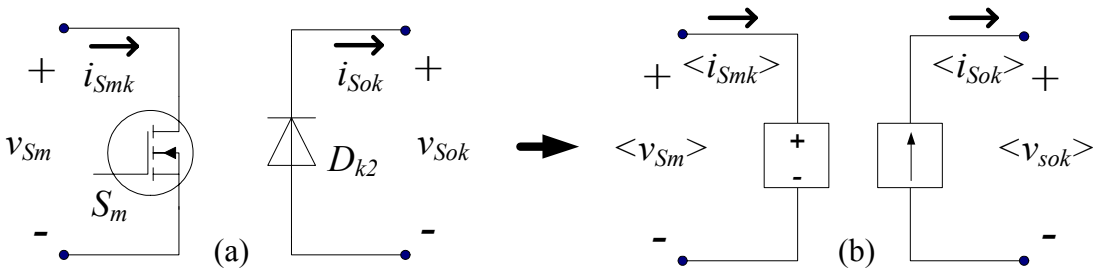


**Figure 3.4:** Defined switch network in the proposed MOFC (a) and equivalent averaged circuit (b) for CCM case.

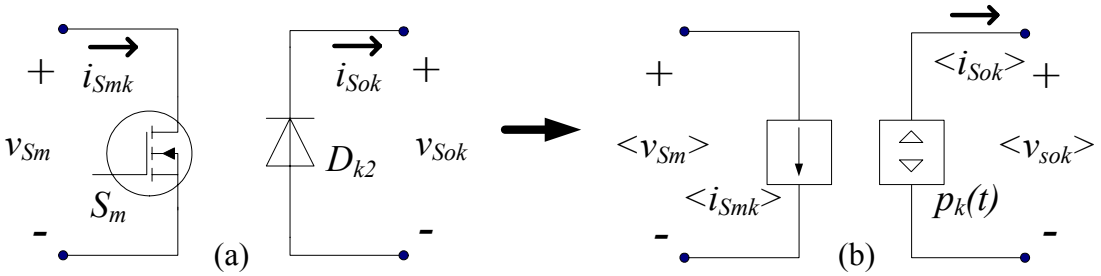


**Figure 3.5:** Defined switch network in the proposed MOFC (a) and equivalent averaged circuit (b) for DCM case.

Figures 3.4 and 3.5 show the defined and equivalent averaged switch circuits for the proposed MOFC. As seen from the figures, in CCM case switch network is represented by dependent voltage and current sources however the switch network is represented by dependent current and power sources for DCM case.

Port quantities of the defined switch network are primary switch current $i_{S_m}$, primary switch voltage $v_{S_m}$, output inductance current $i_{S_{ok}}$ and voltage across the out freewheeling diode $v_{S_{ok}}$. Let *x(t)* be any port quantity, then the averaged form of *x(t)* is given by <*x(t)*> such that

$$< x(t) >= \frac{1}{T_s} \int_{t}^{t+T_s} x(t)dt \tag{3.2}$$

All of the switch network port quantities are also shown in Figure 3.1. Waveforms of the port quantities and magnetizing current of the proposed MOFC are shown in Figure 3.6.

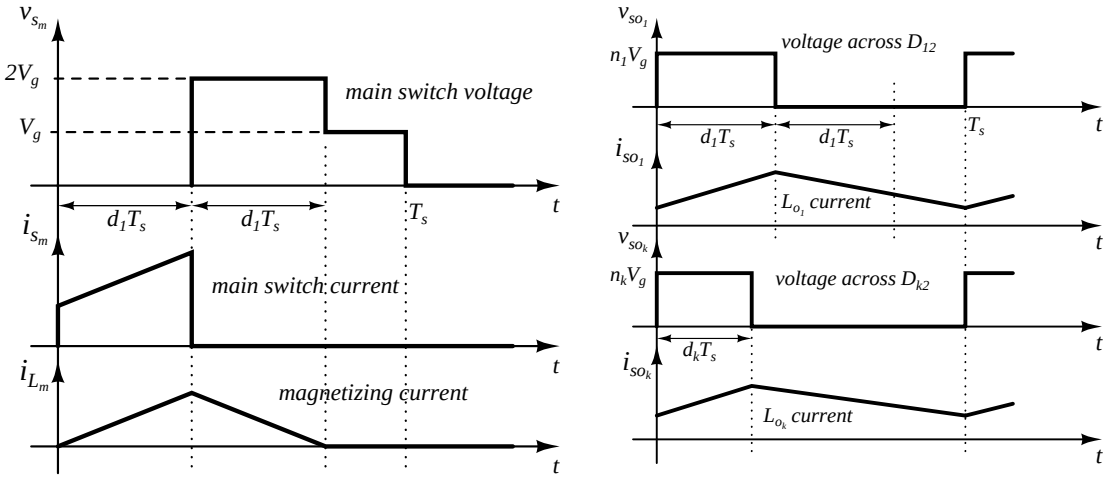


**Figure 3.6:** Key waveforms of the multi-output forward converter for CCM case.

Following assumptions are taken into account during modeling the converter:

I. Source impedance is neglected.
II. There is no any leakage inductance in transformer.
III. Circuit elements and semiconductor switches are ideal.
IV. Duty cycle of the first output is greater than others; $d_1 > d_k$ , $k=2,3,..,n$ . Thus duty cycle of main switch $S_m$ and $S_1$ is the same and equals to $d_1$.

### 3.2.1 Large Signal Model for CCM Case

Analysis is carried out by averaging $i_{S_m}$ , $v_{S_m}$ , $i_{S_{ok}}$ and $v_{S_{ok}}$ waveforms over one switching period as mentioned before. Waveforms given in Figure 3.6 are used for averaging process.

Average value of the primary switch voltage $v_{S_m}$ is:

$$\left\langle v_{S_m} \right\rangle = 2v_g d_1(t) + v_g\left[1 - 2d_1(t)\right] \tag{3.3a}$$

$$\left\langle v_{S_m} \right\rangle = v_g \tag{3.3b}$$

Average value of the primary switch current $i_{S_m}$ is:

$$\left\langle i_{S_m} \right\rangle = \left\langle i_{L_m} \right\rangle + \sum_{k=1}^{n} \left\langle i_{S_k} \right\rangle n_k \tag{3.4a}$$

$$\left\langle i_{S_m} \right\rangle = \left\langle i_{L_m} \right\rangle + \sum_{k=1}^{n} d_k(t) \left\langle i_{S_{ok}} \right\rangle n_k \tag{3.4b}$$

$$\left\langle i_{S_m} \right\rangle = \frac{v_g}{L_m} T_s {d_1}^2(t) + \sum_{k=1}^{n} d_k(t) \frac{v_{ok}}{R_{ok}} n_k \tag{3.4c}$$

Average value of the $k^{th}$ switch network output voltage $v_{S_{ok}}$ is:

$$\left\langle v_{S_{ok}} \right\rangle = n_k v_g d_k(t) \tag{3.5}$$

Average value of the $k^{th}$ switch network output current $v_{S_{ok}}$ is:

$$\left\langle i_{S_{ok}} \right\rangle = I_{ok} = \frac{v_{ok}}{R_{ok}} \tag{3.6}$$

Using (3.3b), (3.4c), (3.5) and (3.6), large signal equivalent circuit of the proposed MFOC can be constructed as in Figure 3.7.

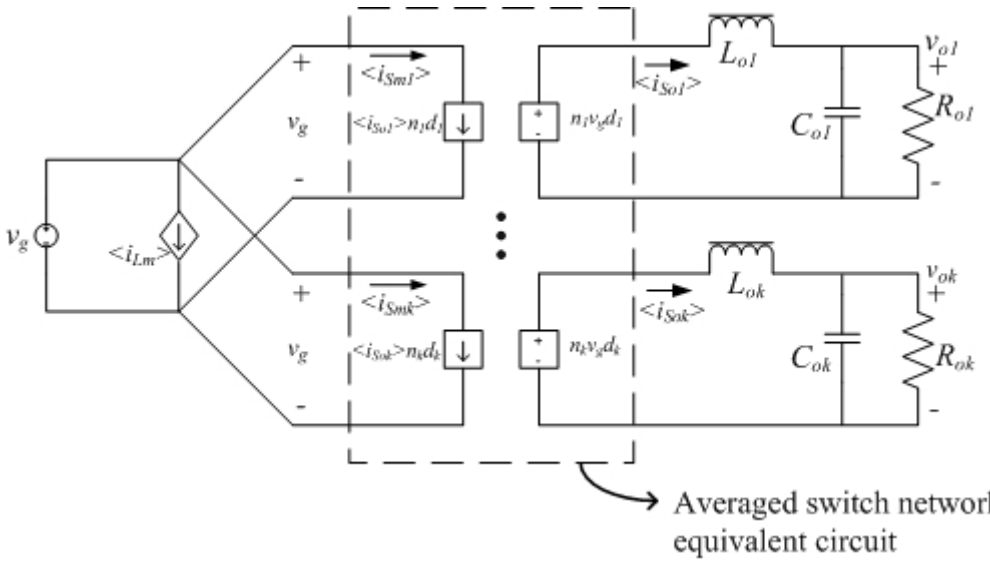


**Figure 3.7:** Large signal equivalent circuit of proposed n-output forward converter for CCM case.

### 3.2.2 Small Signal Model for CCM Case

In order to obtain the small signal model of the proposed multi-output forward converter, averaged switch circuit electrical quantities are perturbed and linearized about a quiescent operating point. Any electrical quantity *x(t)* is written as the

summation of its steady-state value and a very small sinusoidal signal superimposed on it:

$$x(t) = X + \hat{x}(t) \tag{3.7}$$

Where $X$ is the steady-state value of $x$ and $\hat{x}$ is the small signal part of $x$. Then, each $x(t)$ in the mathematical model is replaced with (3.7) and only first order small signal terms are taken into account. Thus, small signal or linear ac equivalent circuit of the converter can be obtained.

Perturbation of input voltage $v_g(t)$ is:

$$v_g = V_g + \hat{v}_g \tag{3.8}$$

Perturbation of duty cycle parameter corresponding to $k^{th}$ output $d_k(t)$ is:

$$d_k = D_k + \hat{d}_k \tag{3.9}$$

Using the result given in (3.3b), small signal equivalent of the main or primary switch voltage is obtained as below:

$$\begin{aligned} \left\langle v_{S_m} \right\rangle &= V_{S_m} + \hat{v}_{S_m} \\ v_g &= V_g + \hat{v}_g \\ \left\langle v_{S_m} \right\rangle &= v_g \Rightarrow \hat{v}_{S_m} = \hat{v}_g \end{aligned} \tag{3.10}$$

Perturbation of main or primary switch current is:

$$\left\langle i_{S_m} \right\rangle = I_{S_m} + \hat{i}_{S_m} \tag{3.11a}$$

and using the result given by (3.4c)

$$\left\langle i_{S_m} \right\rangle = I_{S_m} + \hat{i}_{S_m} = \left( \frac{V_g + \hat{v}_g}{L_m} \right) \left( D_1 + \hat{d}_1 \right)^2 + \sum_{k=1}^{n} \left( D_k + \hat{d}_k \right) \left( I_{S_{ok}} + \hat{i}_{S_{ok}} \right) n_k \tag{3.11b}$$

If the first order terms of the equation (3.11b) are taken into account and the higher order terms are ignored, small signal equivalent of the main switch current is

$$\hat{i}_{S_m} = \frac{2V_g T_s D_1}{L_m}\hat{d}_1 + \frac{{D_1}^2 T_s}{L_m}\hat{v}_g + \sum_{k=1}^{n} I_{S_{ok}} n_k \hat{d}_k + n_k D_k \hat{i}_{S_{ok}} \tag{3.12}$$

This result can also be written in a parametric form like below

$$\hat{i}_{S_m} = j_m \hat{d}_1 + \frac{1}{R_m}\hat{v}_g + \sum_{k=1}^{n} j_k \hat{d}_k + \sum_{k=1}^{n} g_k \hat{i}_{S_{ok}} \tag{3.12b}$$

where

$$\begin{aligned} j_m &= \frac{2V_g T_s D_1}{L_m} \\ R_m &= \frac{L_m}{{D_1}^2 T_s} \\ j_k &= I_{S_{ok}} n_k, k = 1,2,...n \\ g_k &= n_k D_k, k = 1,2,...n \end{aligned} \tag{3.13}$$

Perturbation of averaged output current of the switch network is:

$$\left\langle i_{S_{ok}} \right\rangle = I_{S_{ok}} + \hat{i}_{S_{ok}} \tag{3.14}$$

Perturbation of averaged output voltage of the switch network is:

$$\left\langle v_{S_{ok}} \right\rangle = V_{S_{ok}} + \hat{v}_{S_{ok}} \tag{3.15}$$

and using the results given in (3.5) and (3.9)

$$\left\langle v_{S_{ok}} \right\rangle = V_{S_{ok}} + \hat{v}_{S_{ok}} = n_k \left(V_g + \hat{v}_g\right)\left(D_k + \hat{d}_k\right) \tag{3.16}$$

If the first order terms of the equation (3.16) are taken and the higher order terms are ignored, small signal equivalent of the switch network's output voltage corresponding to $k^{th}$ output is

$$\hat{v}_{S_{ok}} = n_k D_k \hat{v}_g + n_k V_g \hat{d}_k \tag{3.17}$$

Using the equations (3.8) to (3.17) small signal equivalent circuit of the proposed MOFC can be shown as in Figure 3.8, where the small signal voltage and current quantities are identified with underlines.

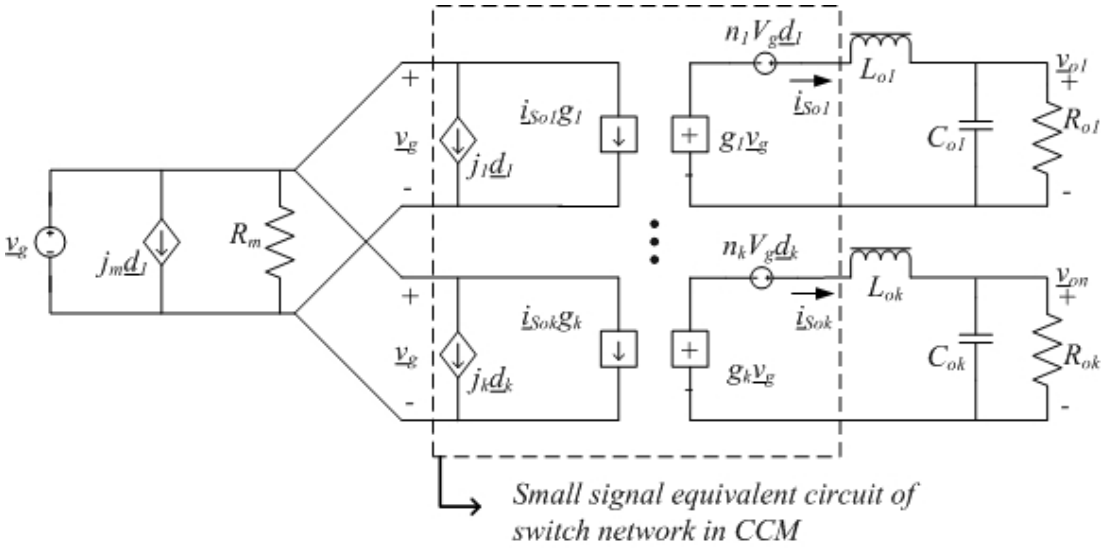


**Figure 3.8:** Small signal equivalent circuit of proposed n-output forward converter for CCM case.

### 3.2.3 Transfer Functions for CCM Case

After obtaining the small signal equivalent circuit of the converter, it is easy to derive the necessary transfer functions to control the converter. Applying basic circuit analysis methods to linear time-invariant circuit given in Figure 3.8 gives rise to any desired input-output relation.

In this section line-to-output, control-to-output transfer functions and the output impedance of the proposed converter are given.

#### 3.2.3.1 Line to Output Transfer Function

Line to output transfer function, the relation between input (source) voltage and the $k^{th}$ output voltage, is defined as:

$$G_{vg_k}(s) = \frac{v_{ok}(s)}{v_g(s)}\Big|_{d_k(s)=0} \tag{3.18}$$

Let $Z_{k1}$ and $Z_{k2}$ are defined as below:

$$Z_{k1}(s) = sL_{ok} \tag{3.19}$$

$$Z_{k2}(s) = \frac{1}{sC_{ok}} // R_{ok} = \frac{R_{ok}}{1 + sR_{ok}C_{ok}} \tag{3.20}$$

As can be easily seen from Figure 3.8

$$G_{vg_k}(s) = \frac{v_{ok}(s)}{v_g(s)} = g_k \frac{Z_{k2}}{Z_{k1} + Z_{k2}} = n_k D_k \frac{Z_{k2}}{Z_{k1} + Z_{k2}} \tag{3.21a}$$

$$G_{vg_k}(s) = \frac{v_{ok}(s)}{v_g(s)} = n_k D_k \frac{1}{s^2 L_{ok} C_{ok} + s\frac{L_{ok}}{R_{ok}} + 1} \tag{3.21b}$$

(3.21) can be written in a more general or design oriented form:

$$G_{vg_k}(s) = \frac{v_{ok}(s)}{v_g(s)} = G_{vg_k}(0) \frac{1}{\left(\frac{s}{\omega_{ok}}\right)^2 + \frac{s}{Q_k \omega_{ok}} + 1} \tag{3.22}$$

where

$$\begin{aligned} G_{vg_k}(0) &= n_k D_k \\ \omega_{ok} &= \frac{1}{\sqrt{L_{ok} C_{ok}}} \\ Q_k &= R_{ok} \sqrt{\frac{C_{ok}}{L_{ok}}} \end{aligned} \tag{3.23}$$

### 3.2.3.2 Control to Output Transfer Function

Control to output transfer function, the relation between the duty cycle and the $k^{th}$ output voltage, is defined as:

$$G_{vd_k}(s) = \frac{v_{ok}(s)}{d_k(s)} \Big|_{v_g(s)=0} \tag{3.24}$$

From the output voltage loop equation of the $k^{th}$ output:

$$G_{vd_k}(s) = \frac{v_{ok}(s)}{d_k(s)} = n_k V_g \frac{Z_{k2}}{Z_{k1} + Z_{k2}} \tag{3.25a}$$

$$G_{vd_k}(s) = \frac{v_{ok}(s)}{d_k(s)} = n_k V_g \frac{1}{s^2 L_{ok} C_{ok} + s\frac{L_{ok}}{R_{ok}} + 1} \tag{3.25b}$$

As it can be seen from (3.21b) and (3.25b), $G_{vd_k}(s)$ has the same zero and poles of $G_{vg_k}(s)$. The only difference between them is the DC gain. So;

$$G_{vd_k}(s) = \frac{v_{ok}(s)}{d_k(s)} = G_{vd_k}(0) \frac{1}{\left(\frac{s}{\omega_{ok}}\right)^2 + \frac{s}{Q_k \omega_{ok}} + 1} \tag{3.26}$$

where $G_{vd_k}(0) = n_k V_g$ and $Q_k$ and $\omega_{ok}$ are given as in (3.23).

#### 3.2.3.3 Output Impedance in CCM

Output impedance of the $k^{th}$ output is defined as:

$$Z_{ok}(s) = \frac{v_{ok}(s)}{i_{ok(s)}} \tag{3.27}$$

while $v_g(s)=0$ and $d_k(s)=0$.

From the Figure 3.8, output impedance corresponding to $k^{th}$ output can be written as the parallel combination of load resistance, output filter capacitance and output inductance such that;

$$Z_{ok}(s) = \frac{v_{ok}(s)}{i_{ok(s)}} = R_{ok} \,//\, \frac{1}{sC_{ok}} \,//\, sL_{ok} \tag{3.26a}$$

$$Z_{ok}(s) = \frac{v_{ok}(s)}{i_{ok(s)}} = \frac{s}{s^2 C_{ok} + s\frac{1}{R_{ok}} + \frac{1}{L_{ok}}} \tag{3.26b}$$

### 3.2.4 Large Signal Model for DCM Case

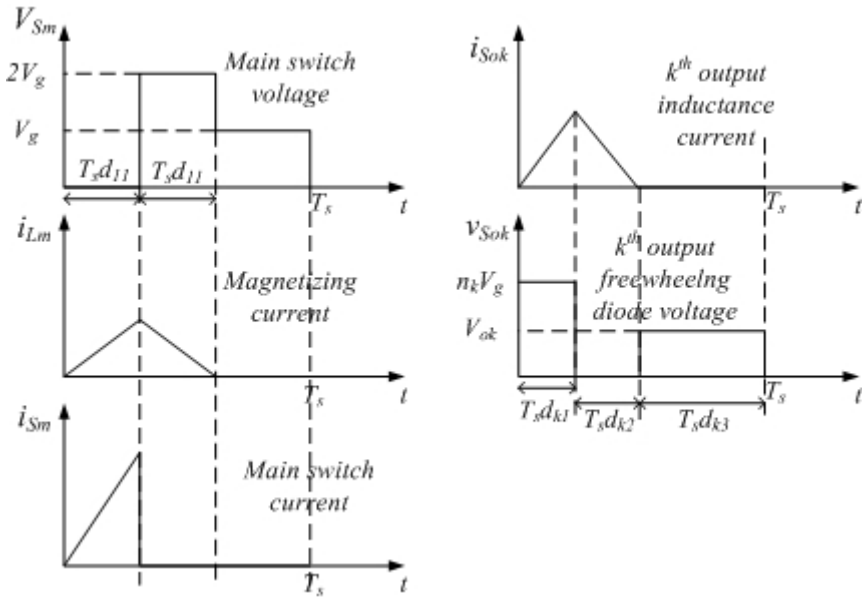


**Figure 3.9:** Key waveforms of the multi-output forward converter for DCM case.

Voltage and current waveforms of the switch network in DCM case are shown in Figure 3.9. Modeling approach in DCM case is similar to that of CCM case. Here again the switch network port quantities are averaged over one period and resulting time-invariant equivalent circuits are used in place of actual switching structure. Analysis is carried out by averaging $i_{Sm}$, $v_{Sm}$, $i_{Sok}$ and $v_{Sok}$ waveforms over one switching period. Waveforms given in Figure 3.9 are used for averaging process.

Average value of the primary switch voltage $v_{Sm}$ is:

$$\left\langle v_{S_m} \right\rangle = 2v_g d_{11}(t) + v_g \left[1 - 2d_{11}(t)\right] = v_g \tag{3.27}$$

Average value of the primary switch current $i_{Sm}$ is:

$$\left\langle i_{S_m} \right\rangle = \left\langle i_{L_m} \right\rangle + \sum_{k=1}^{n} \left\langle i_{S_k} \right\rangle n_k \tag{3.28a}$$

$$\left\langle i_{S_m} \right\rangle = \frac{v_g {d_{11}}^2 T_s}{L_m} + \sum_{k=1}^{n} n_k \frac{n_k v_g - v_{ok}}{R_{ek}} \tag{3.28b}$$

$$\left\langle i_{S_{mk}} \right\rangle = n_k \frac{n_k v_g - v_{ok}}{R_{ek}} \tag{3.28c}$$

where

$$R_{ek} = \frac{2L_{ok}}{{d_{k1}}^2 T_s} \tag{3.29}$$

Average value of the k[th] switch network output voltage $v_{So_k}$ is:

$$\left\langle v_{S_{ok}} \right\rangle = n_k v_g d_{k1} + v_{ok}\left(1 - d_{k1} - d_{k2}\right) \tag{3.30a}$$

$$\left\langle v_{S_{ok}} \right\rangle = n_k v_g d_{k1} + v_{ok}\left(1 - d_{k1}\frac{n_k v_g}{v_{ok}}\right) = v_{ok} \tag{3.30b}$$

$$\left\langle v_{S_{ok}} \right\rangle = v_{ok} \tag{3.30c}$$

where

$$d_{k2} = \frac{n_k v_g - v_{ok}}{v_{ok}} d_{k1} \tag{3.31}$$

Average value of the $k^{th}$ switch network output current $i_{So_k}$ is:

$$\left\langle i_{S_{ok}} \right\rangle = \frac{n_k v_g - v_{ok}}{R_{ek}} \frac{n_k v_g}{v_{ok}} \tag{3.32a}$$

$$\left\langle i_{S_{ok}} \right\rangle = \left\langle i_{S_{mk}} \right\rangle \frac{v_g}{v_{ok}} \tag{3.32b}$$

Using (3.27) to (3.32), large signal equivalent circuit of the proposed MFOC for DCM case can be constructed as in Figure 3.10.

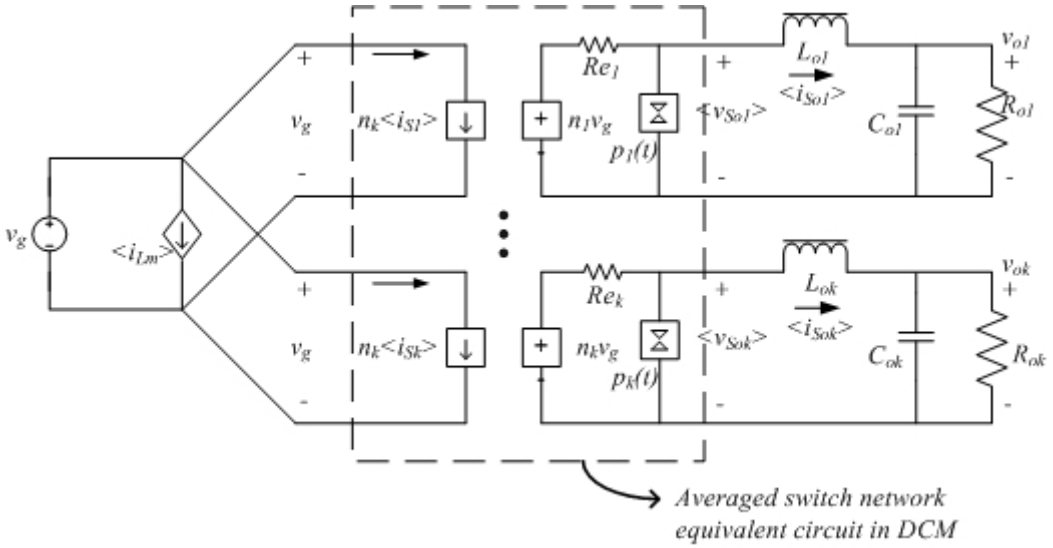


**Figure 3.10:** Large signal equivalent circuit of proposed n-output forward converter for DCM case.

### 3.2.5 Small Signal Model for DCM Case

Small signal parameters of the proposed MOFC for DCM case are found in a similar way as in CCM case. However, this time after perturbing the each averaged electrical quantity, small signal parameters can be determined by taking the three dimensional Taylor series of magnetizing current $<i_{Lm}>$, primary switch current $<i_{Smk}>$ and output inductance current $<i_{Sok}>$.

Figure 3.11 shows the equivalent small signal circuit of the proposed multi output forward converter. In that figure, small signal quantities are shown with underlines. Using classical circuit analysis method desired transfer functions of the converter system can be obtained.

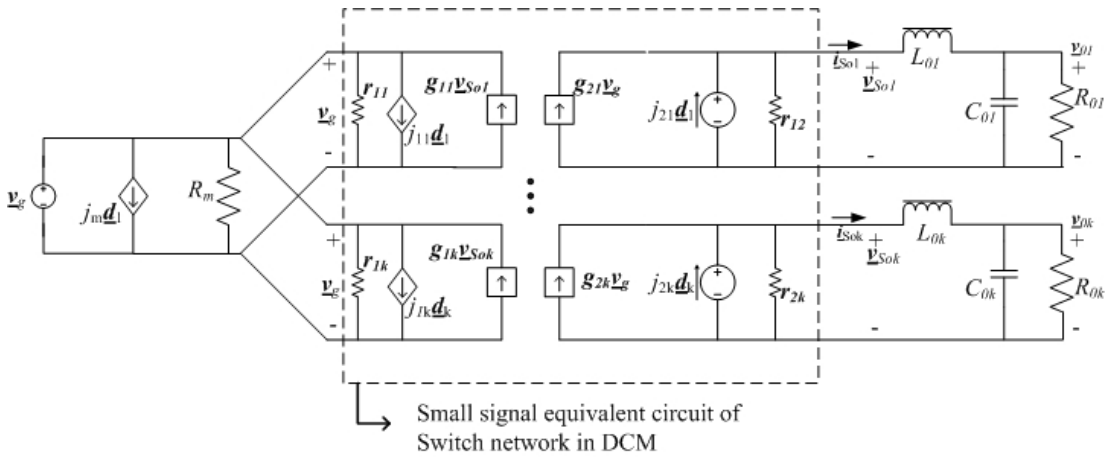


**Figure 3.10:** Small signal equivalent circuit of proposed n-output forward converter for DCM case.

Table 3.1 summarizes the small signal parameters where k represent the output number, k = 1,2,..,n:

**Table 3.1:** Small signal parameters of MOFC for DCM case

| $g_{1k}$ | $j_{1k}$ | $r_{1k}$ | $g_{2k}$ | $j_{2k}$ | $r_{2k}$ | $j_m$ | $R_m$ |
|---|---|---|---|---|---|---|---|
| $\frac{n_k}{R_{ek}}$ | $\frac{{n_k}^2 2V_g(1-M_k)}{D_k R_{ek}}$ | $\frac{R_{ek}}{{n_k}^2}$ | $\frac{n_k(2-M_k)}{M_k R_{ek}}$ | $\frac{n_k 2V_g(1-M_k)}{M_k D_k R_{ek}}$ | $R_{ek}{M_k}^2$ | $\frac{2V_g D_k T_s}{L_m}$ | $\frac{L_m}{{D_k}^2 T_s}$ |

where $D_k$ is the duty cycle of the MOSFET being at the $k^{th}$ output, $T_s$ is switching period and $R_{ek}$ was given in (3.29). $M_k$ is the dc conversion ratio between supply voltage and k$^{th}$ output and is given by;

$$M_k = \frac{V_{ok}}{n_k V_g} = \frac{2}{1+\sqrt{1+\frac{4R_{ek}}{R_{ok}}}} \tag{3.33}$$

### 3.2.6 Transfer Functions for DCM Case

In this section line-to-output, control-to-output transfer functions and the output impedance of the proposed converter are given for DCM case.

#### 3.2.6.1 Line to Output Transfer Function

Solving the circuit given in Figure 3.10 line to output transfer function of the converter for the k$^{th}$ output is obtained as below where $d_k(s) = 0$:

$$G_{vg_k}(s) = \frac{v_{ok}(s)}{v_g(s)}\Big|_{d_k(s)=0} = g_{2k}\left[r_{2k} \,//\, \frac{1}{sC_{ok}} \,//\, R_{ok}\right] \tag{3.34}$$

If (3.34) is written in a more general or design oriented form:

$$G_{vg_k}(s) = G_{vg_k}(0)\frac{1}{1+\left(\frac{s}{\omega_{pk}}\right)} \tag{3.35}$$

where

$$
\begin{aligned}
&G_{vg_k}(0) = n_k M_k \\
&\omega_{pk} = \frac{2 - M_k}{(1 - M_k) R_{ok} C_{ok}} \\
&M_k = \frac{2}{1 + \sqrt{1 + \frac{4R_{ek}}{R_{ok}}}} = \frac{2}{1 + \sqrt{1 + \frac{8L_{ok}}{D_k{}^2 T_s R_{ok}}}}
\end{aligned}
\tag{3.36}
$$

### 3.2.6.2 Control to Output Transfer Function

Similarly control to output transfer function of the converter system can be obtained solving output voltage loop equation of the circuit given in Figure 3.10 by letting $v_g(s) = 0$.

$$
G_{vd_k}(s) = \frac{v_{ok}(s)}{d_k(s)}\Big|_{v_g(s)=0} = j_{2k}\left[ r_{2k} \,//\, \frac{1}{sC_{ok}} \,//\, R_{ok} \right] \tag{3.37}
$$

If (3.35) is written in a more general or design oriented form:

$$
G_{vg_k}(s) = G_{vg_k}(0) \frac{1}{1 + \left( \frac{s}{\omega_{pk}} \right)} \tag{3.38}
$$

where

$$
\begin{aligned}
&G_{vd_k}(0) = n_k \frac{2V_g}{D_k} \frac{1 - M_k}{2 - M_k} \\
&\omega_{pk} = \frac{2 - M_k}{(1 - M_k) R_{ok} C_{ok}} \\
&M_k = \frac{2}{1 + \sqrt{1 + \frac{4R_{ek}}{R_{ok}}}} = \frac{2}{1 + \sqrt{1 + \frac{8L_{ok}}{D_k{}^2 T_s R_{ok}}}}
\end{aligned}
\tag{3.39}
$$

### 3.2.6.3 Output Impedance in DCM

Output impedance of the k[th] output is defined as:

$$Z_{ok}(s) = \frac{v_{ok}(s)}{i_{ok(s)}}\Bigg|_{v_g(s)=0, d_k(s)=0} \tag{3.40}$$

From the Figure 3.10, output impedance corresponding to k[th] output can be written as the parallel combination of load resistance, output filter capacitance and output inductance in series with $r_{2k}$ such that;

$$Z_{ok}(s) = \frac{v_{ok}(s)}{i_{ok(s)}} = R_{ok} \,//\, \frac{1}{sC_{ok}} \,//\, (r_{2k} + sL_{ok})$$

$$Z_{ok}(s) = \frac{s\left(\frac{L_{ok}R_{ok}}{R_{ok}+r_{2k}}\right) + \frac{R_{ok}r_{2k}}{R_{ok}+r_{2k}}}{s^2\left(\frac{L_{ok}R_{ok}C_{ok}}{R_{ok}+r_{2k}}\right) + s\left(\frac{L_{ok}+R_{ok}C_{ok}r_{2k}}{R_{ok}+r_{2k}}\right) + 1} \tag{3.41}$$

Dc gain of $Z_{ok}(s)$ is

$$Z_{ok}(0) = R_{ok} \,//\, r_{2k} = \frac{R_{ok}r_{2k}}{R_{ok}+r_{2k}} = \frac{R_{ok}(1-M_k)}{2-M_k} \tag{3.42}$$

It is seen from (3.42) that, forward converter operating in DCM case has a finite output impedance comparable with load impedance at steady state.

## 4. SIMULATION RESULTS

In this section, proposed concept for independent and precise regulation of MOFCs is verified by computer simulation. Control method developed for n-output forward converter is applied to two output case. The two output forward converter shown in Figure 4.1 has the following specifications:

- Output 1: 5V, 0-10A, 50W
- Output 2: 12V, 0-4A, 48W
- Switching Frequency : 20 kHz
- Input Voltage: 42V ±10V DC.

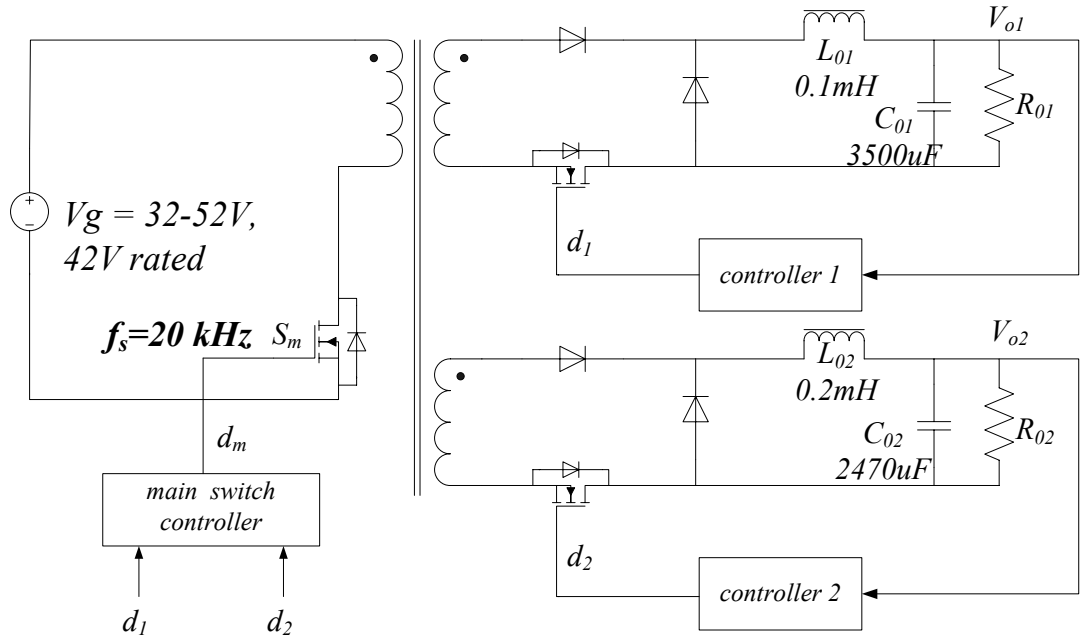


**Figure 4.1:** Two-output forward converter which is simulated with proposed control scheme.

PSIM simulation software is used through simulations. The output inductance and capacitor values for 5V-output are respectively $L_{01}$ = 0.1mH and $C_{01}$ = 3500uF. On the other hand, the output inductance and capacitor values for 12V-output are

respectively $L_{02}$ = 0.2mH and $C_{02}$ = 2470uF. Determination of those values is explained in Appendix B.

### 4.1 Line Regulation of the MOFC with Proposed Concept

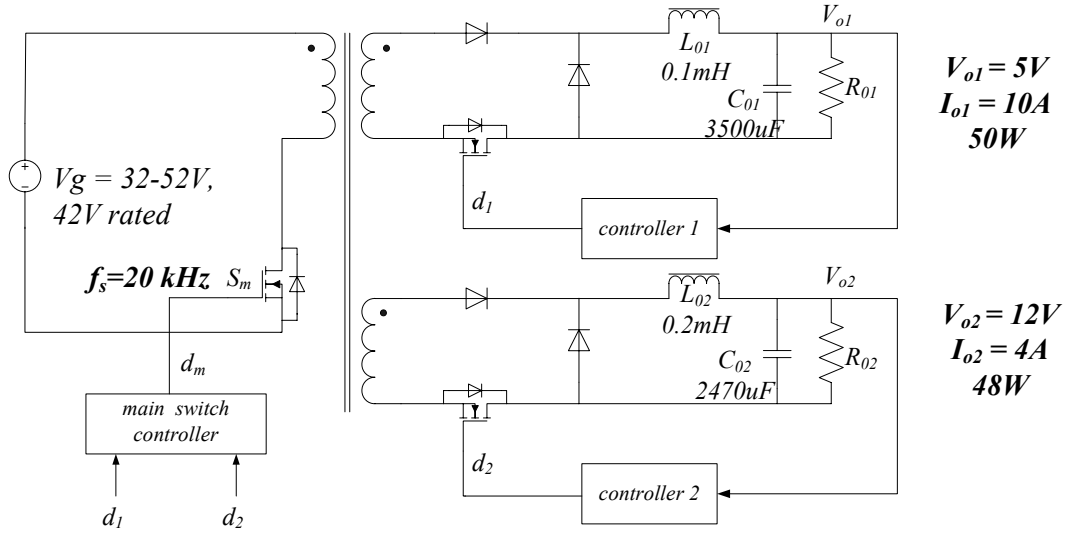


**Figure 4.2:** Two-output forward converter for line regulation test.

Figure 4.2 shows the power stage of the forward converter that is under line regulation test. Input voltage is first changed from 42V to 52V, than from 52V to 32V, while both outputs are at their full loads (10A and 4A respectively) during the simulation. Figure 4.3 shows the input voltage variation during simulation.

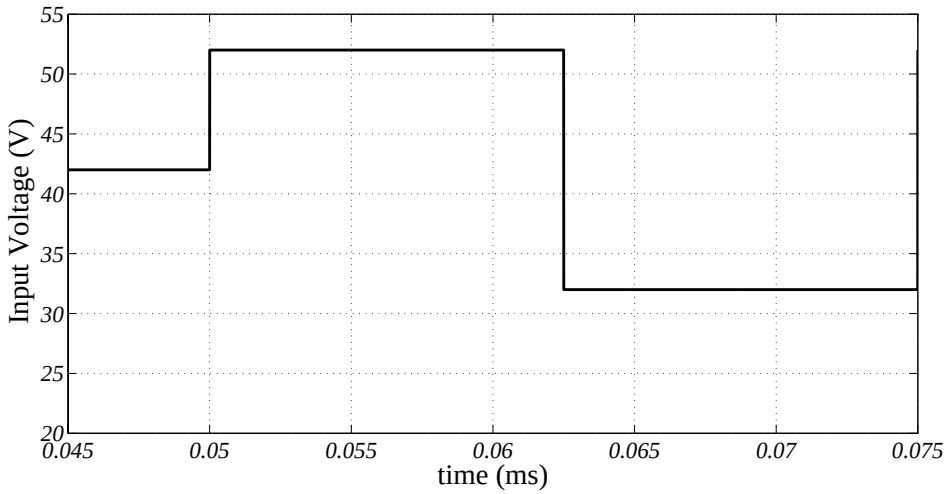


**Figure 4.3:** Change of input voltage during line regulation test.

Figure 4.4 shows the line regulation of the converter controlled by the proposed concept. Although neither current mode control nor input voltage feed-forward control method is used, line regulations of outputs are satisfactory for given line variation at full load operation. Because of the proposed concept, regulation of the two output forward converter against line variations is very good such that each output is regulated independently and precisely as seen in Figure 4.4.

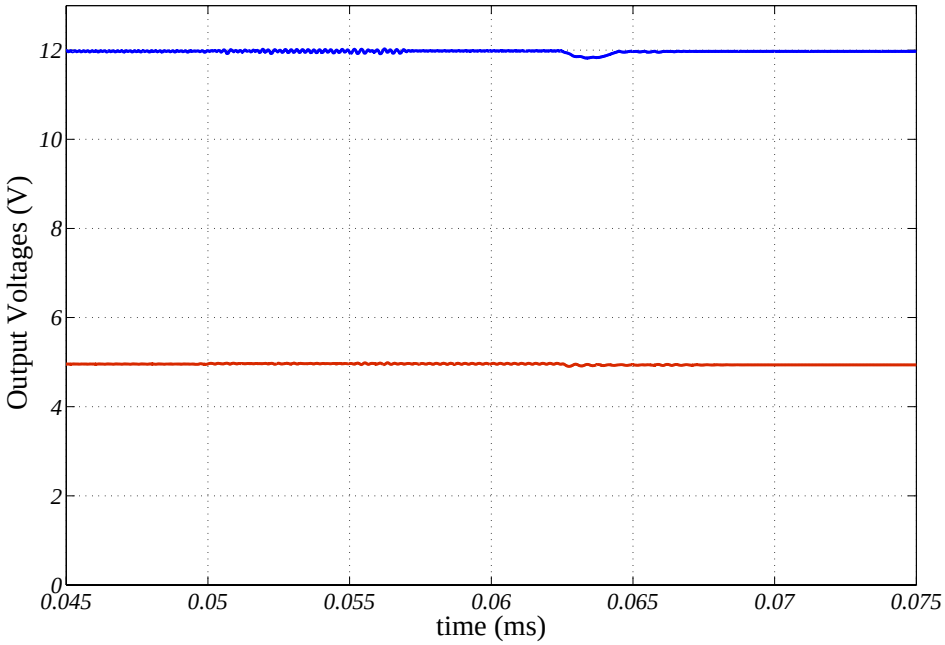


**Figure 4.4:** Regulations of output voltages against line variations.

### 4.1.1 Some Key Waveforms of the Two-Output Forward Converter with Proposed Control Concept

In this part, some important waveforms are given which were defined as switch network quantities during modeling section. Besides that, duty cycle variations of the main and the output switches are also introduced to show the principle of the proposed control method.

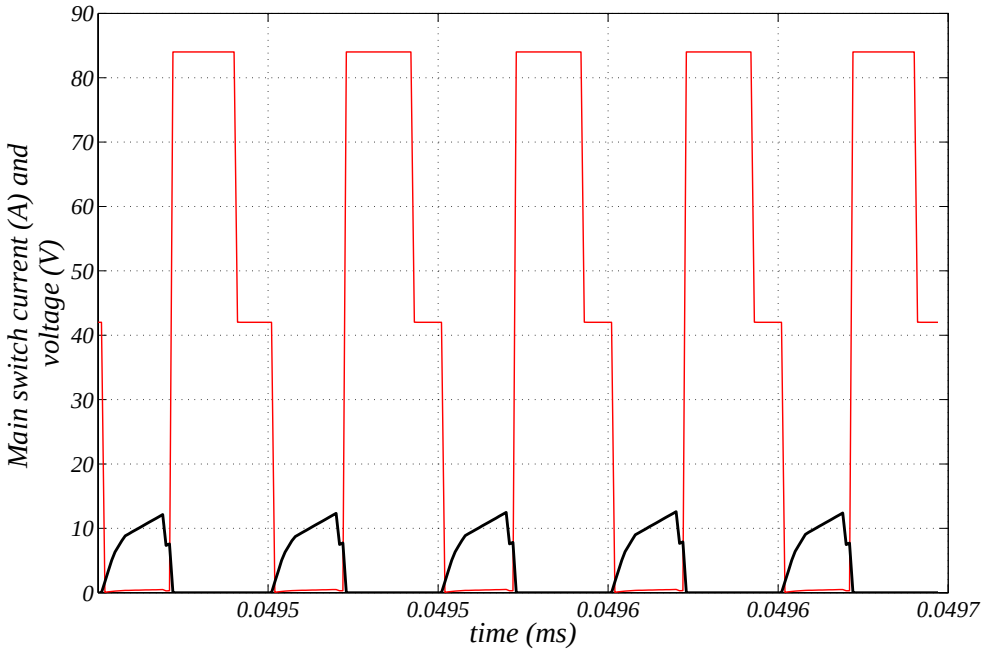


**Figure 4.5:** Main switch current and voltage waveforms

Figure 4.5 shows the current and voltage waveforms, primary MOSFET current and drain to source voltage, for the main switch which are the input port quantities of the switch network defined in Section 3.2. Input voltage is 42V and held constant. On the other hand, output currents are also at rated values (10A for 5V-output, 4A for 12V-output) during the simulation.

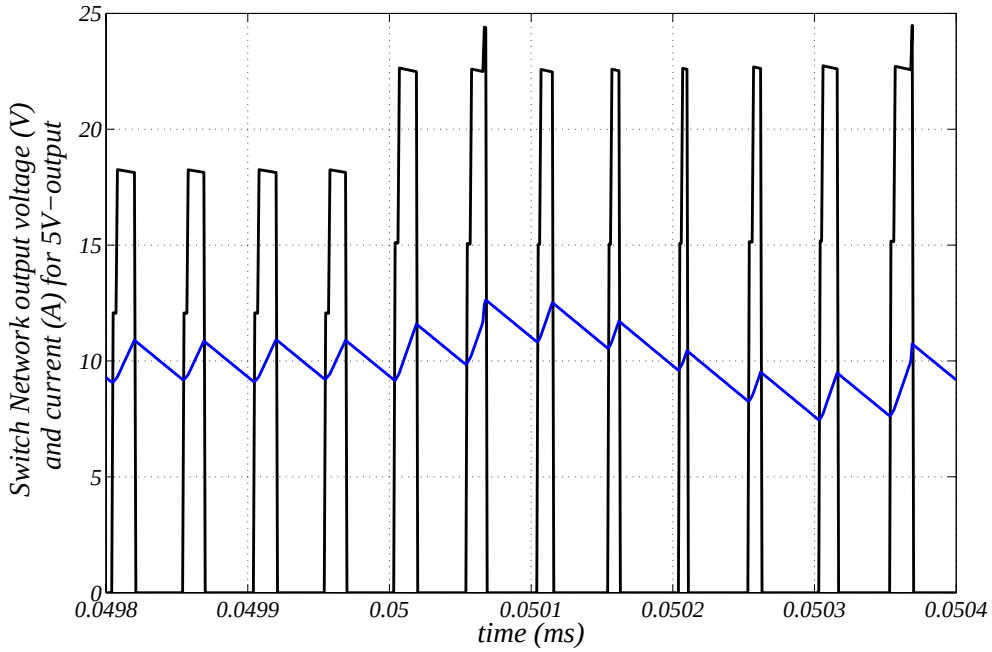


**Figure 4.6:** Switch network output current and voltage waveforms for 5V-output.

Figure 4.6 shows the switch network output current and voltage waveforms, output inductance current and cathode voltage of the freewheeling diode, for 5V-output. During the simulation input voltage is 42V firstly, then at the instant of 0.05ms input voltage is suddenly changed to 52V. Output currents are at their rated values, 10A for 5V-output, 4A for 12V-output during that simulation.

Similarly Figure 4.7 shows the switch network output current and voltage waveforms, output inductance current and cathode voltage of the freewheeling diode, for 12V-output. Simulation conditions are the same of the case for 5V-output.

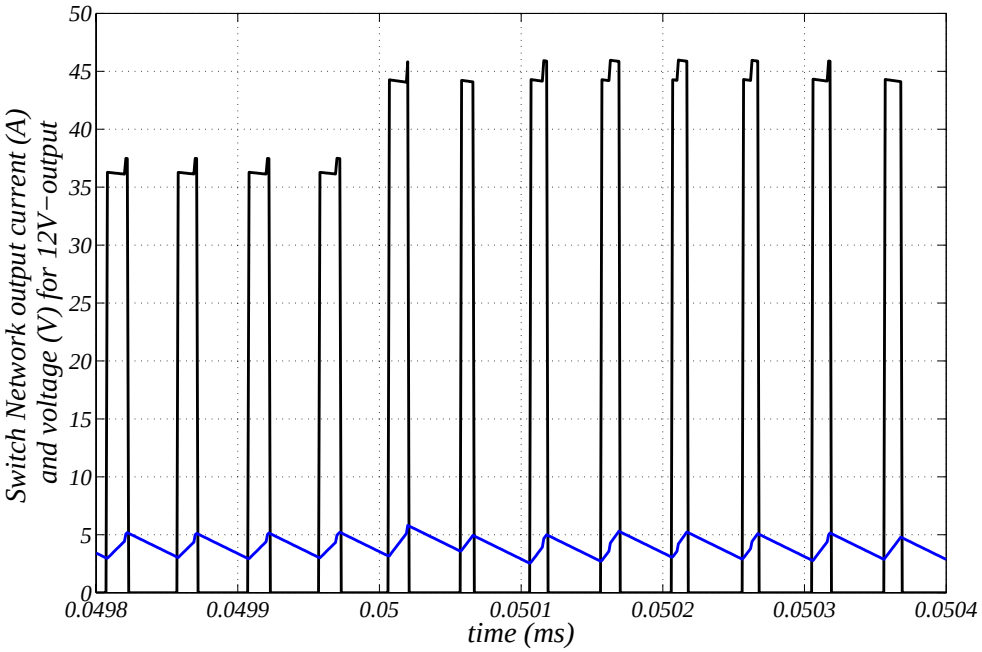


**Figure 4.7:** Switch network output current and voltage waveforms for 12V-output.

Figure 4.8 shows gating signals of output switches for 5V and 12V-outputs in the same time interval (from 0.0498ms to 0.0504ms) in which switch network waveforms are given as in Figure 4.6 and 4.7. The red signal is the gating signal of the 5V-output switch and the blue one is the gating signal of the 12V-output switch.

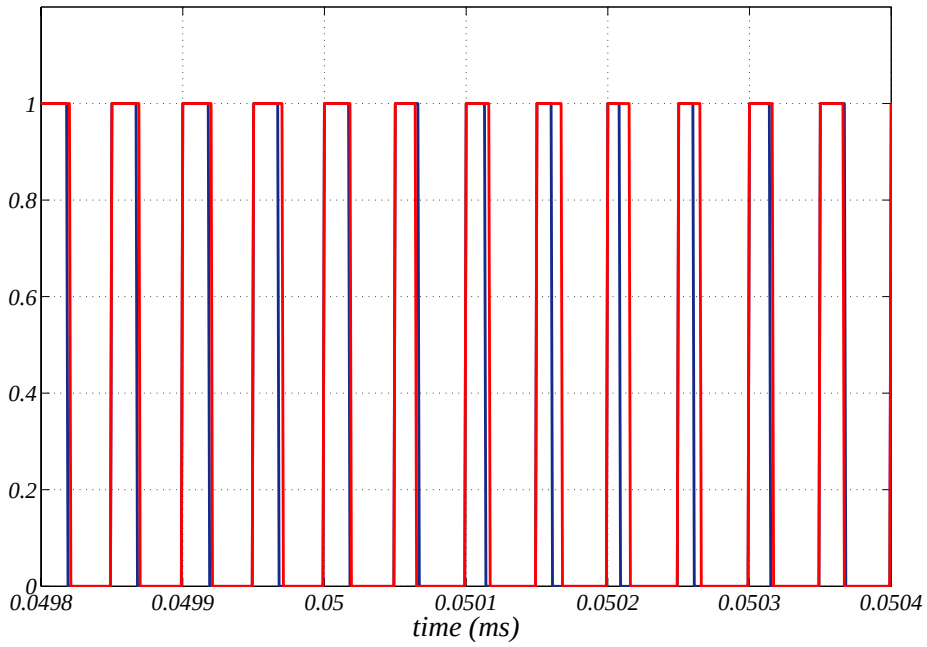


**Figure 4.8:** Gating signals of the output switches

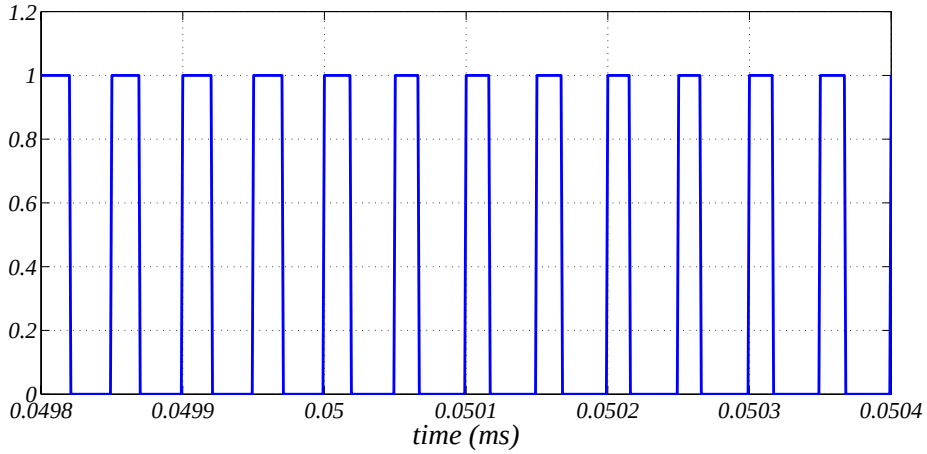


**Figure 4.9:** Gating signals of the main switch

Figure 4.9 shows the gating signal and duty cycle variation of the main switch. As mentioned in section 3.1, main switch gating signal is obtained as the ORing of output gating signals.

## 4.2 Load Regulation of the MOFC with Proposed Concept

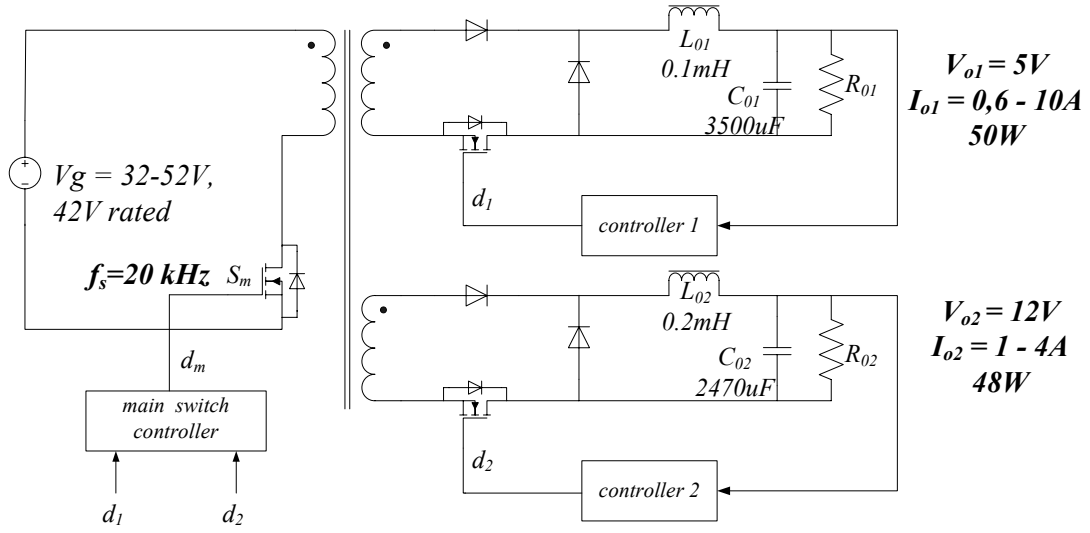


**Figure 4.10:** Two-output forward converter for load regulation test

Figure 4.10 shows the power stage of the forward converter which is under load regulation test. During the load regulation tests input voltage is kept constant at 42V. As a first case, 5V output current is changed from 0.6A (DCM operation) to 10A (CCM operation) and than back to 0.6A again. Similarly 12V output current is

changed from 0.8A (DCM operation) to 4A (CCM operation) and than back to 0.8A again with a small time delay according to 5V output current. Change of output currents and the responses of output voltages to those variation are shown in Figure 4.11 and 4.12 respectively.

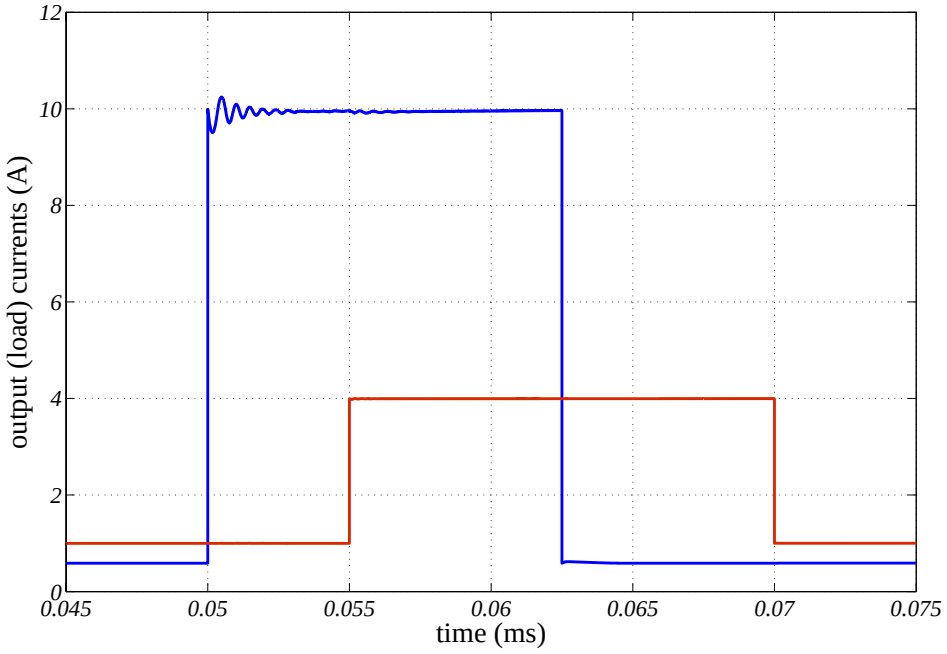


**Figure 4.11:** Variations of output currents during load regulation tests

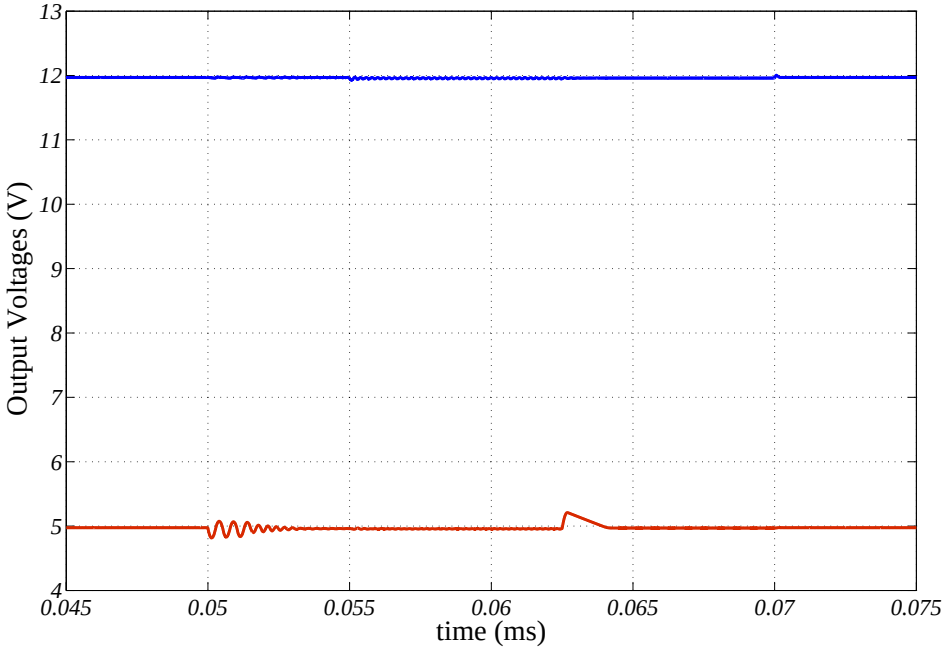


**Figure 4.12:** Load regulation of the output voltages under proposed control method.

As seen from Figure 4.12, cross coupling between outputs is eliminated greatly and each output voltage is regulated independently and precisely. Load change of any output does not affect the voltage of other output. Figure 4.13 and 4.14 shows the variations of 5V-output and 12V-output voltages respectively in detail. Load regulation at both outputs is below 4%.

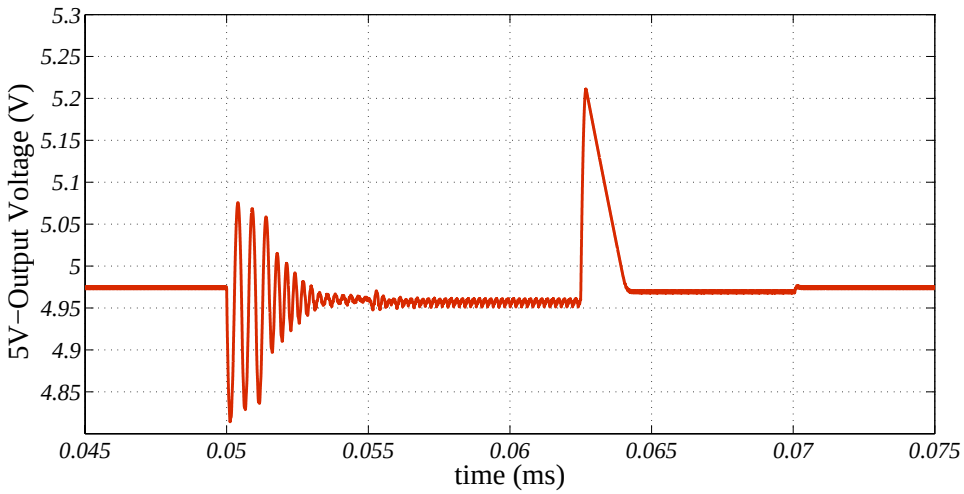


**Figure 4.13:** Close view of the 5V-output voltage waveform during load regulation test

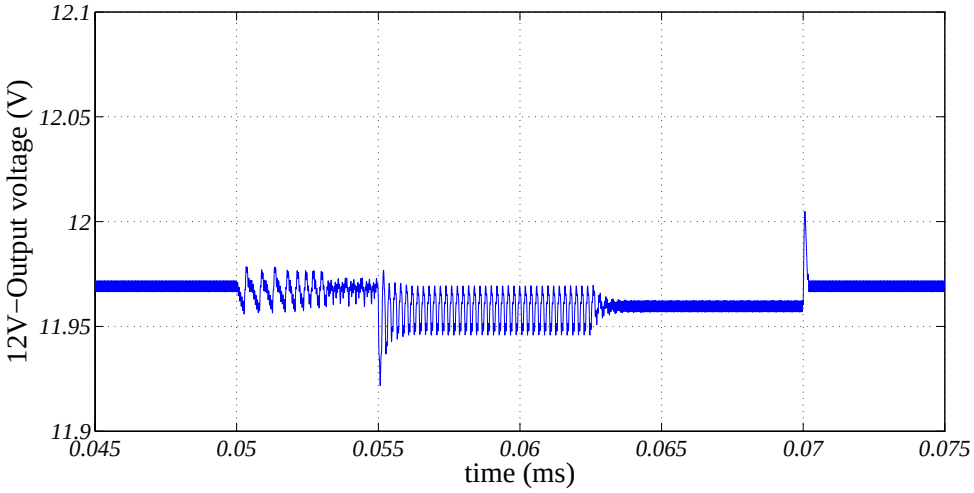


**Figure 4.14:** Close view of the 12V-output voltage waveform during load regulation test

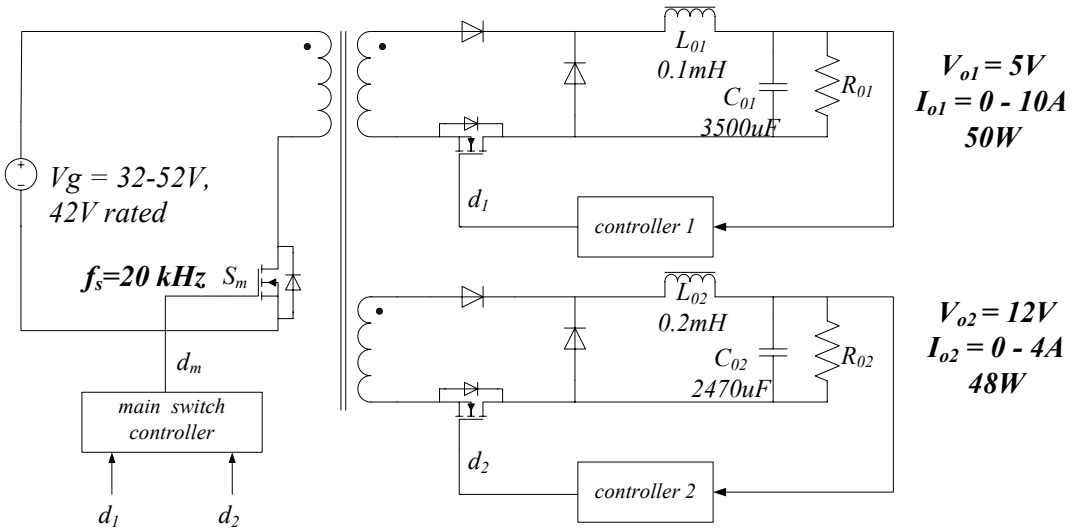


**Figure 4.15:** Two-output forward converter for load regulation test (from no-load to full-load variation case)

Figure 4.15 shows the power stage of the forward converter of which load regulation test is carried out for the case of no-load to full-load variation of output currents. Input voltage is kept constant at 42V during the simulation. 5V-output current is stepwise changed from 0A (no load) to 10A (full load) than back to 0A. 12V-output current is stepwise changed from 0A (no load) to 4A (full load) than back to 1A again with a time delay with respect to 5V-output current. Figure 4.16 shows the variations of output currents during simulation.

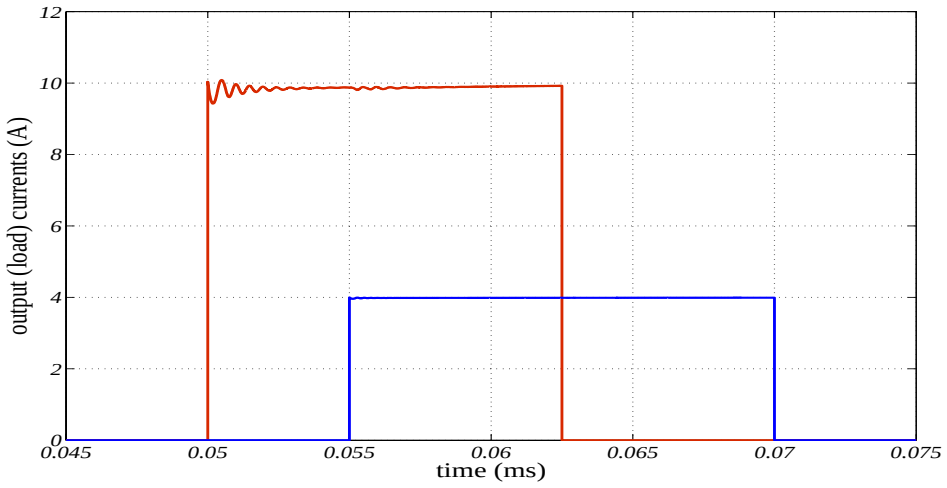


**Figure 4.16:** Variations of output currents during load regulation tests (from no-load to full-load)

Figure 4.17 and 4.18 shows the variations of 5V-output and 12V-output voltages respectively in detail. As can be seen from the figures, regulation of any output is totally independent from others.

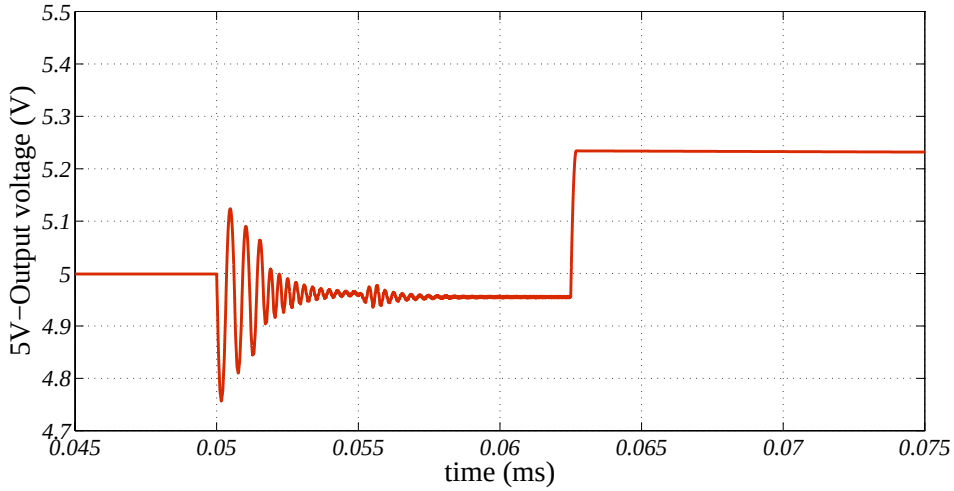


**Figure 4.17:** Close view of the 5V-output voltage waveform during load regulation test (from no-load to full-load)

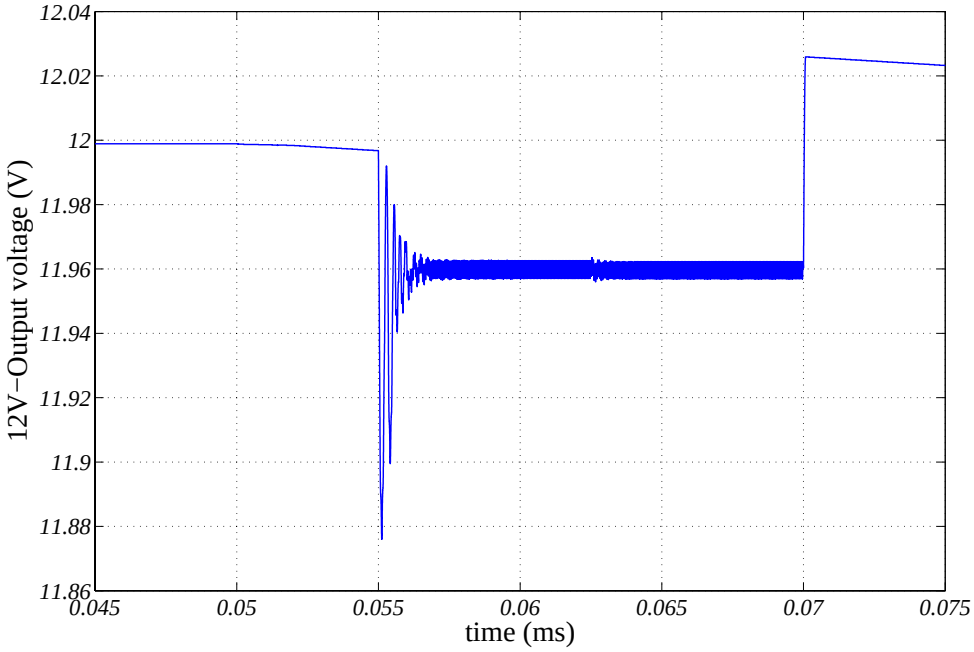


**Figure 4.18:** Close view of the 12V-output voltage waveform during load regulation test (from no-load to full-load)

### 4.3 Load Regulation of the Two-Output Forward Converter with Conventional Master Slave Based Control

In this section, the same two-output forward converter is simulated under conventional master-slave based control method to show the effectiveness and success of the proposed control method. Similar load regulation tests are applied to forward converter controlled conventionally and results are presented. Figure 4.19 shows the two-output forward converter in which only 5V-output is controlled (master-output) and 12V-output is the slave-output.

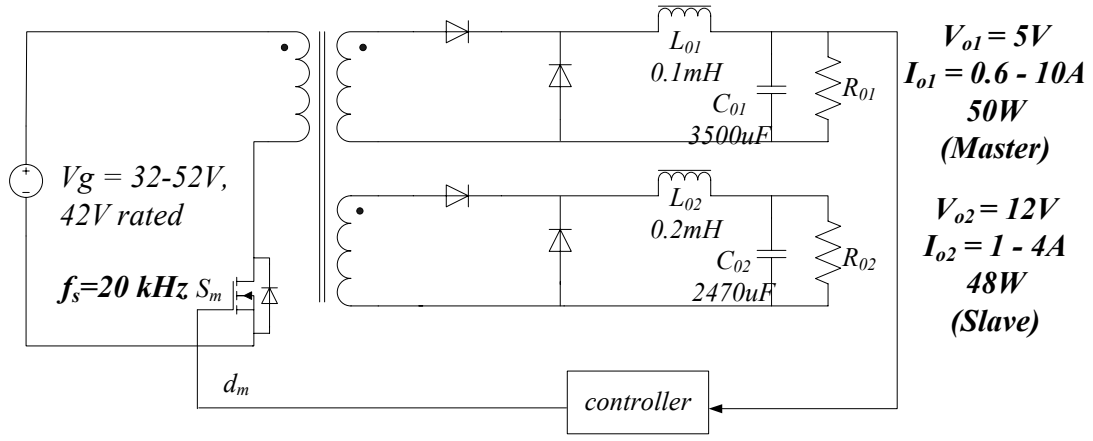


**Figure 4.19:** Two-output forward converter with master-slave based control method

As a first case, 5V-output current is changed from 0.6A (DCM) to 10A (CCM) then back to 0.6A while input voltage is kept constant at 42V. Figure 4.20 and 4.21 shows the variations of output currents and output voltages respectively. As seen from Figure 4.20; while 5V-outout is well regulated, there is a steady state error which can not be ignored at 12V-output at both 0.6A and 10A operation of the 5Voutput. On the other hand, during the load changes in master output, the slave output deviates much more from 12V. However, 12V-output does not loose its regulation completely when 5V-output operates at light load because there is a small load (or dummy load) at 5V-output.

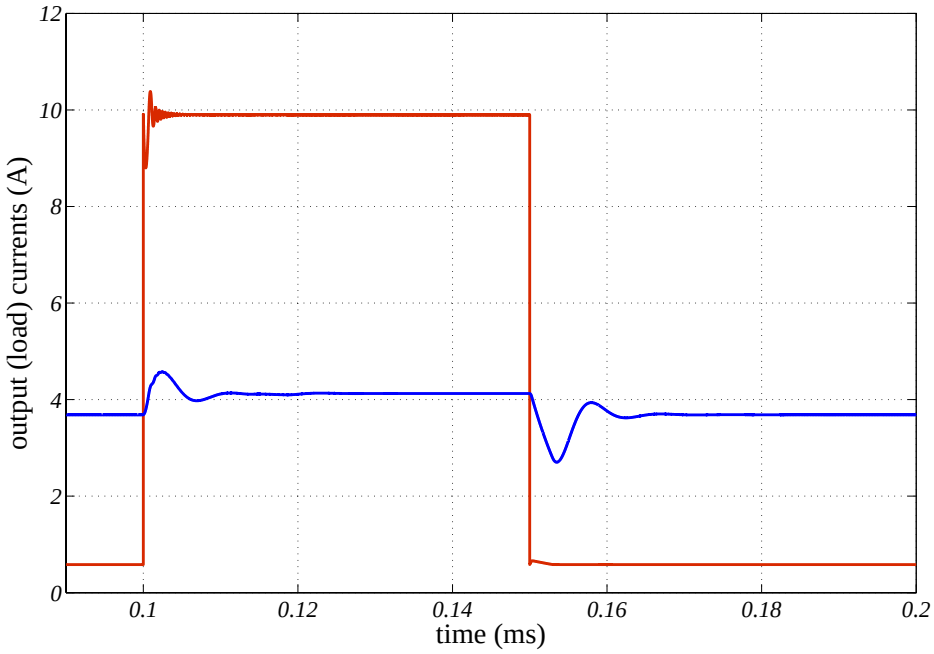


**Figure 4.20:** Variation of 5V (red) and 12V-output (blue) currents in master-slave based forward converter.

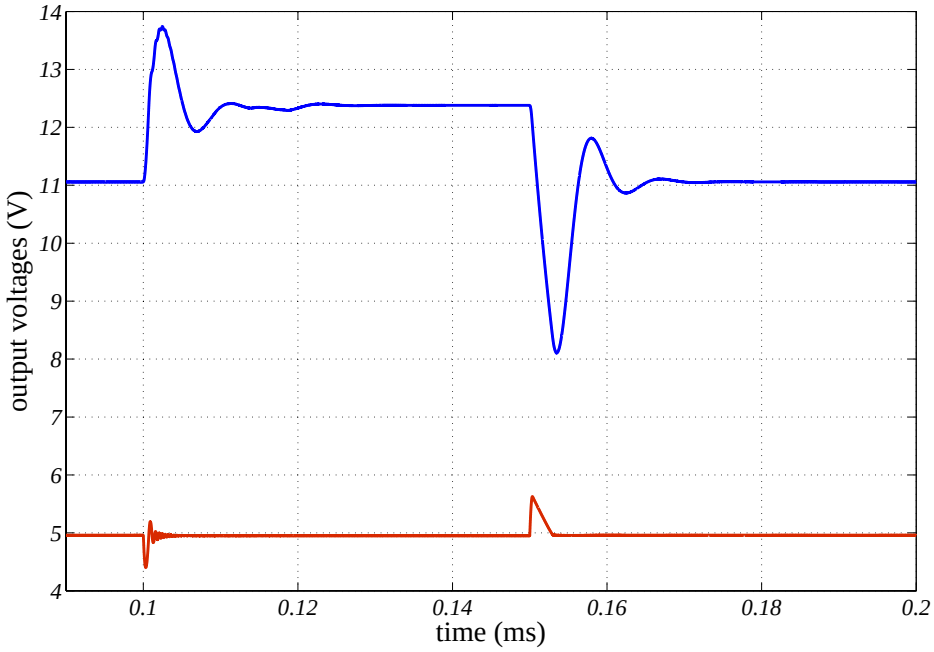


**Figure 4.21:** Variation of 5V (red) and 12V-output (blue) voltages in master-slave based forward converter.

Another simulation case investigated for the load regulation of the conventionally controlled forward converter is the no-load operation of the main output while the slave output is at its full-load. Figure 4.22 shows the output current variations of the converter and Figure 4.23 shows the corresponding output voltage variations.

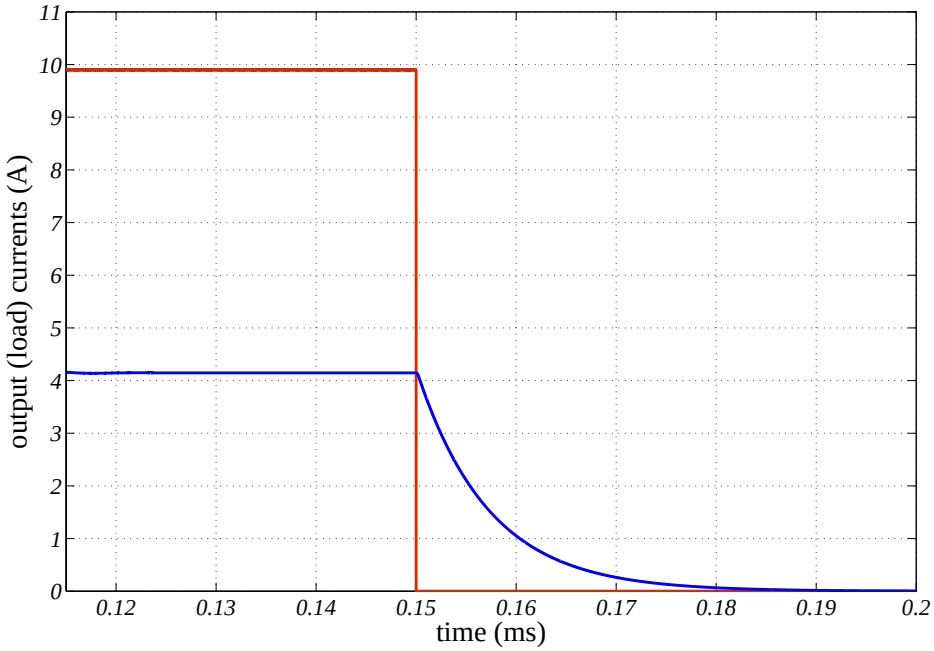


**Figure 4.22:** Variation of 5V (red) and 12V-output (blue) currents in master-slave based forward converter; master-output goes from full-load to no-load.

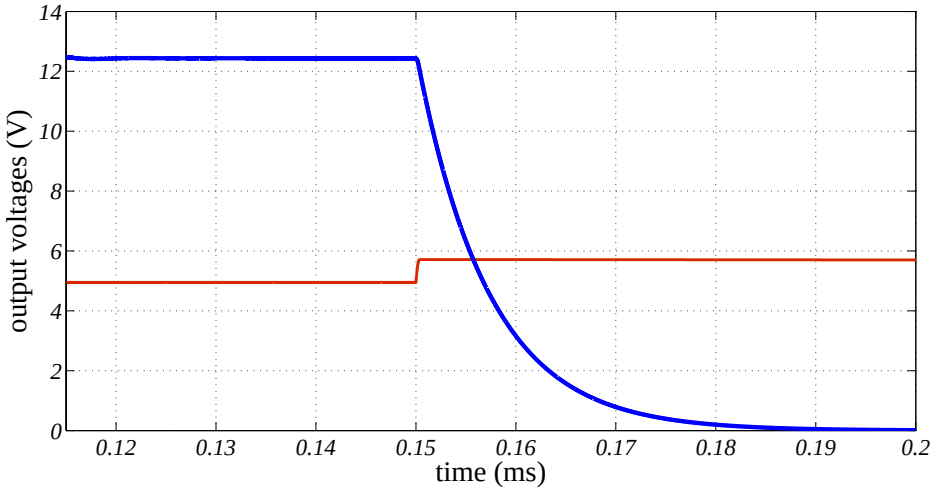


**Figure 4.23:** Variation of 5V (red) and 12V-output (blue) voltages in master-slave based forward converter; master-output goes from full-load to no-load.

As can be seen from Figure 4.23, when the master-output operates at no-load, slave-output completely looses its regulation. Te reason of that situation is that; because master-output power decreases to zero, the controller reduces to duty cycle of the main switch nearly to zero. As a result of this, the slave-output experiences lack of power and loose its voltage regulation.

Another simulation case investigated for the load regulation of the conventionally controlled forward converter is the no-load operation of the slave-output while the master-output is at its full-load. Figure 4.24 shows the output current variations of the converter and Figure 4.25 shows the corresponding output voltage variations.

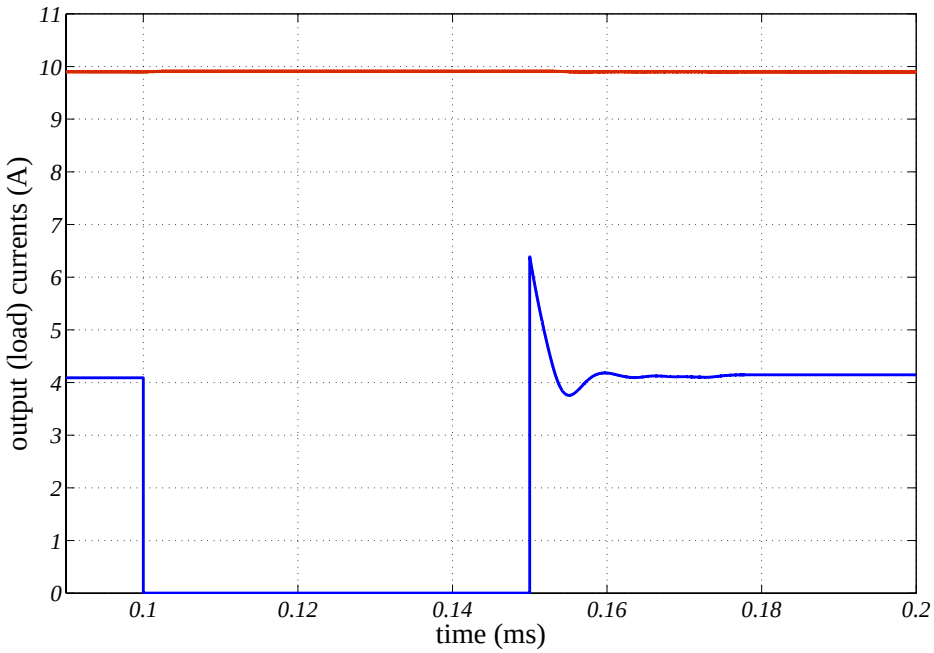


**Figure 4.24:** Variation of 5V (red) and 12V-output (blue) currents in master-slave based forward converter; slave-output goes from full-load to no-load.

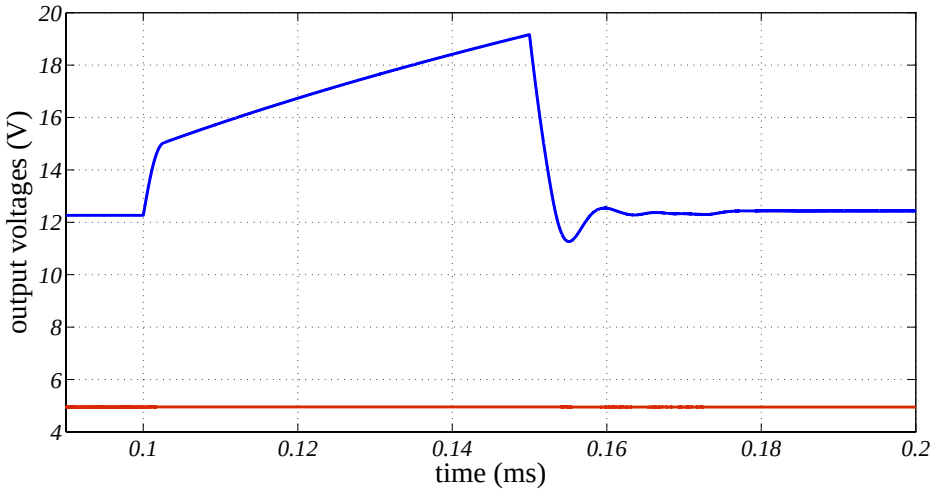


**Figure 4.25:** Variation of 5V (red) and 12V-output (blue) voltages in master-slave based forward converter; slave-output goes from full-load to no-load.

## 5. CONCLUSION and FUTURE WORKS

In this study, a new concept combining post and pre-regulation to obtain independent and precise regulation in multi-output forward converters is introduced. Proposed method modifies conventional forward converter topology by adding extra controlled switches to outputs. Duty cycles of each output are determined by widely known method which is the comparison of a sawtooth signal and the compensated error signal. However, each output's compensated error signal is compared with a common sawtooth carrier such that all of the gating signals are synchronized. Assigning a dedicated controller for each output, duty cycle of each output are decoupled from each other. Primary switch's duty cycle information is extracted from output duty cycle values with a very simple rule which is just selecting the maximum output duty cycle as the primary switch's duty cycle. Combination of the topological modification and easy control rule produced a simple but a novel control method for multi-output forward converters.

For generality n-output forward converter with proposed control scheme has been modeled based on averaged switch model described in [16]. Decoupling the duty cycles of each output showed that n-output forward converter can be represented by n-number of paralleled forward converter fed by the same voltage source. Detailed large and small signal equivalent circuits of the proposed converter were derived for both CCM and DCM cases. Line-to-output and control-to-output transfer functions and output impedances of the proposed converter has been reported for both CCM and DCM cases.

A two-output, 42V to 5V-10A and 12V-4A, forward converter was designed for application of the proposed method. Simulation results for two-output forward converter have verified the explained concept.

Simulation results showed that line regulation of the two-output forward converter is also excellent.

Simulation results also showed that proposed method removes cross coupling between different outputs and provides precise voltage regulation independent from operation mode of any output(s). Any output may be either in CCM or DCM. The load regulation of the converter is excellent. Any output even may operate at no load without loosing the voltage regulation. So there is no need to dummy load for auxiliary outputs as is for conventional master-slave based multi-output forward converters.

Simplicity of topology and control scheme allows large number of output designs without difficulty.

Control scheme can be realized in analog or digital fashion and may be implemented as PWM IC easily. However, it is more suitable for DSP or microcontroller implementation for hardware simplicity.

Disadvantages of the proposed method are the requirement of n number of additional forward path diodes for each output circuit and the providing common sawtooth carrier for isolated output circuits. There is not a directly usable PWM integrated circuit in the market. In case of isolated outputs, an optocoupler for each output and an additional optocoupler for primary switch is required. That is, totally n+1 number of optocouplers are required for n-output forward converter.

As far as investigated proposed method is the simplest and one of the most effective solutions for the regulation problem of multi-output forward converters in the literature. Table 5.1 compares the control schemes and converters proposed in literature.

**Tablo 5.1:** Comparison of proposed converters in the literature

| Scheme | Magnetics | Cross Regulation | Complexity |
|---|---|---|---|
| Magamp Post Regulator | 1 transformer and (1 saturable reactor + 1 inductor) per output | Good in narrow range but poor in wide load ranges | High |
| WVMC | 1 transformer + 1 inductor per output | Acceptable in narrow load ranges but poor in wide load ranges | Very Low |
| Parallel Regulation Method | 1 transformer + 1 inductor per output, +1 inductor per auxiliary output | Good in moderate range but, "?" in wide load ranges | Very High |
| SSPR | 1 transformer + 1 inductor per output | Good in narrow load ranges but, "?" in wide load ranges | Moderate |
| Time Shared Controlled Current Source | Only one inductor is shared amongst the outputs (non-isolated case) | Good in wide load ranges | Moderate |
| Voltage Feed Forward Synchronous Forward Converter | 1 transformer, 2 inductor per output | Good in wide load ranges | Moderate |
| Synchronous Forward Converter with Auomatic Master-Slave Assignment | 1 transformer, 2 inductor per output | Good in wide load ranges | Moderate |
| Proposed converter in this work | 1 transformer + 1 inductor per output | Good in wide load ranges | Low |

Future works for this study can be summarized as below:

- Analog and DSP based implementation of the proposed converter in order to verify the concept experimentally.
- Application of the proposed concept to non-isolated multi-output dc-dc converters.
- Integration with alternative controllers such as current mode control, digital dead-beat control, fuzzy control…etc.

## REFERENCES


[1] **Wen Chau-Chun, Chen Chem-Lin, Chen Wei, Jiary Jian,** " Magamp Post Regulation for Flyback Converter", IEEE, 2001.

[2] **Milan M. Jovanovic, Laszio Huber,** "Small-Signal Modeling of Magamp PWM Switch", *Applied Power Electronics Conference*, pp. 922-928, 1997.

[3] **J. Lee, D. Y. Chen, Y. P. Wu, C. Jamerson,** "Modeling of Control Loop Behavior of Magamp Post Regulators", *IEEE International Telecommunications Energy Conf (INTELEC) Proc*., Paper 20.1, 1989.

[4] **Robert M. Tedder,** "Limitations of the Magamp Regulator and an Improved Magamp Choke Design Procedure", *Applied Power Electronics Conference*, pp. 109-117, 1988.

[5] **Robett M. Tedder,** "Effects of Converter Type, Reset Method and Core Material on Magamp Regulator Performance", *Applied Power Electronics Conference*, pp. 391-400, 1989.

[6] **J. Lee, D. Y. Chen, C. Jamerson,** "Magamp Post Regulators-Practical Design Considerations to Allow Operation Under Extreme Loading Conditions", *IEEE Transactions on Power Electronics*, Vol. 5, No. 1, pp.69-76, 1990.

[7] **Y. Chen, D. Chen, Y. Wu**, "Conrol-Loop Modelling of Multiple Output Feedback of Forward Converters", *IEEE Transactions on Power Electronics*, Vol.8, No. 3, pp. 320-328, July 1993.

[8] **Chen Qing, Lee Fred C.,** Jovanovic Milan M., "Current Mode Control for Multiple-Output Converters", *IEEE Transactions on Aerospace and Electronic Systems*", Vol. 32, No. 4, pp:1412 – 1420, October 1996.

[9] **Chen, Q., Lee, F.C., Jovanovic,** M.M., "Analysis and Design of Weighted Voltage Mode Control for a Multi-Output Forward Converter", *Applied Power Electronics Conference and Exposition*, pp:449 – 455, 7-11 March 1993.

[10] **Ferreres, A., Carrasco, J.A., Espi, J.M., Casans, S., Dede, E.J.,** "Modeling of a Novel Parallel Regulation Technique in a Two Output Forward Converter", *IEEE International Symposium on Industrial Electronics*, Vol. 2, pp:607 – 612, 12-16 July 1999.

[11] **Lin Y., Liu K.H.,** "A New Synchronous Switch Post Regulator for Multi Output Forward Converters", *APEC'90*, pp.693-696, 1990.

[12] **Chakraborty S., Jain A. K., Mohan N.,** "A Novel Converter Topology for Multiple Individually Regulated Outputs", *IEEE Transactions on Power Electronics*, Vol.21, No.2, 2006.

[13] **Xi Yauhao, Jain K. Praveen, Liu Y,** "A Precisely Regulated Multiple Output Forward Converter Topology", *Applied Power Electronics Conference and Exposition*, Vol. 2, pp:986 – 992, 2000.

[14] **Xi Yauhao, Jain K. Praveen,** "A Forward Converter Topology With Independently and Precisely Regulated Multiple Outputs", *IEEE Transactions on Power Electronics*, Vol.18, No. 2, pp. 648-658, 2003.

[15] **Xi Yauhao, Jain K. Praveen,** "A Precisely-Regulated Multiple Output Forward Converter with Automatic Master Slave Control", *IEEE 36th Power Electronics Specialists Conference,* pp:969 – 975, 2005.

[16] **Robert W. Erickson,** "Fundamentals of Power Electronics", First Edition, Kluwer Academic Publishers, Massachusetts, 1997.

## APPENDIX A: DETERMINATION of OUTPUT INDUCTANCE and CAPACITOR VALUES

### A.1 Determination of Output Inductance Values

Output inductance value is determined according to the desired amount of the inductance current ripple. Peak-to-peak value of ripple current of the output inductance is given by,

$$\Delta i_k = \left( \frac{n_k V_g - V_{ok}}{L_{ok}} \right) D_k T_s \tag{A.1}$$

$L_{ok}$ value can be calculated using the equation (A.1). $T_s$ is the switching frequency and is 50μs. The approach given below is embraced in order to determine the inductance values:

For 5V-output, it is desired that let the ripple current be $\Delta i_1 = 2A$ when the line voltage is its minimum $V_g = 32V$ and converter operates in CCM-DCM boundary. In this case duty cycle of the 5V-output is

$$D_1 = \frac{V_{o1}}{n_1 V_g} = \frac{5}{\frac{6}{11} \times 32} = 0.286 \tag{A.2}$$

Using (A.1), $L_{o1}$ can be calculated as below

$$L_{o1} = \left( \frac{n_1 V_g - V_{o1}}{\Delta i_1} \right) D_1 T_s = \left( \frac{\frac{6}{11} \times 32V - 5V}{2A} \right) 0{,}287 \times 50.10^{-6} \approx 0.1mH \tag{A.3}$$

For 12V-output, it is desired that let the ripple current be $\Delta i_2 = 2A$ when the line voltage is its minimum $V_g = 32V$ and converter operates in CCM-DCM boundary. In this case duty cycle of the 12V-output is

$$D_2 = \frac{V_{o2}}{n_2 V_g} = \frac{12}{\frac{13}{11} \times 32} = 0.317 \tag{A.4}$$

Using (A.1), $L_{o2}$ can be calculated as below

$$L_{o2} = \left( \frac{n_2 V_g - V_{o2}}{\Delta i_2} \right) D_2 T_s = \left( \frac{\frac{13}{11} \times 32V - 12V}{2A} \right) 0{,}317 \times 50.10^{-6} \approx 0.2mH \tag{A.4}$$

## A.2 Determination of Output Capacitor Values

Output capacitor value is determined according to the desired amount of the output or capacitor voltage ripple. Peak-to-peak value of ripple voltage of the output capacitor is given by,

$$C_{ok} \geq \frac{\Delta Q}{\Delta V_{ok}} \tag{A.5}$$

Here $\Delta Q$ is the amount of charge that capacitor stores or releases during one switching period. Assuming that the ripple current of the output inductor flows through the capacitor, $\Delta Q$ is given by,

$$\Delta Q_k = \Delta i_k \frac{T_s}{4} \tag{A.6}$$

where $k$ = 1,2. Knowing $\Delta i_1 = \Delta i_2 = 2A$, $\Delta Q_k$ values are calculated as

$$\Delta Q_1 = \Delta Q_2 = \Delta i_k \frac{T_s}{4} = 2A \frac{50.10^{-6}\,\text{sec}}{4} = 25.10^{-6}\,A\text{sec} \tag{A.7}$$

Let the ripple voltage of 5V-output be lower than 1%. In this case $C_{o1}$ value should be,

$$C_{o1} \geq \frac{\Delta Q_1}{\Delta V_{o1}} = \frac{25.10^{-6}\,A\text{sec}}{0{,}01.5V} = 500\mu F \tag{A.8}$$

Therefore, 5V-output capacitor value is selected as $C_{o1}$ = 3500μF.

Let the ripple voltage of 12V-output be lower than 1%. In this case $C_{o2}$ value should be,

$$C_{o2} \geq \frac{\Delta Q_2}{\Delta V_{o2}} = \frac{25.10^{-6}\,A\text{sec}}{0{,}01.12V} = 208\mu F \tag{A.9}$$

Therefore, 12V-output capacitor value is selected as $C_{o1}$ = 2470μF.

Selected capacitor values are higher than that of calculated values. The first reason of such selection is that the capacitors should be able to carry the ripple current of the inductor without overheating. The second reason is that during the above calculations it has been assumed also that the series equivalent resistance of the capacitor is negligible. In order to compensate such real world effects, capacitor values should be selected higher than calculated ones.

## APPENDIX B: CONTROLLER DESIGN for TWO-OUTPUT FORWARD CONVERTER

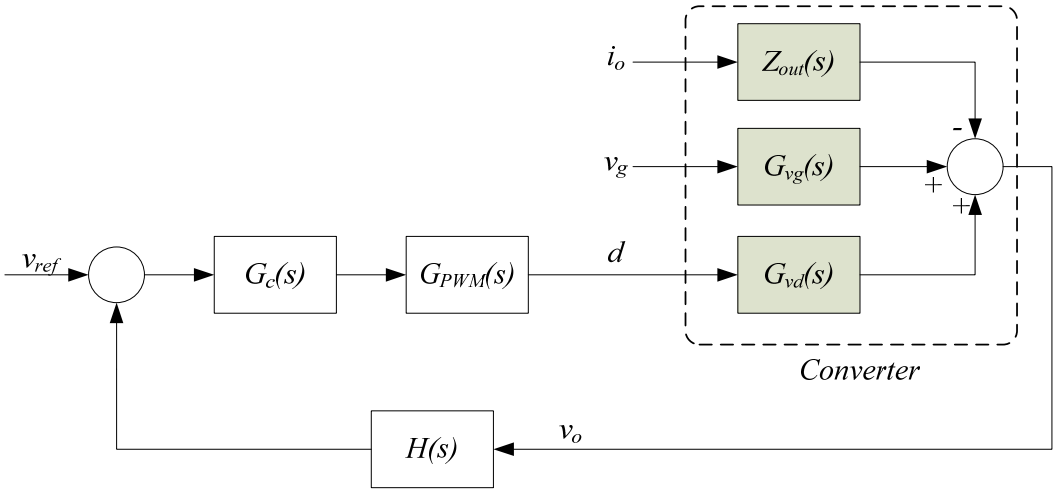


**Figure B.1** Block diagram of forward converter system.

Figure B.1 shows the block diagram of the forward converter system for one output. Design of $G_c(s)$ is based on the conventional linear controller design such as given in [16]. Taking the reference voltage $v_{ref} = 5V$, sensor gain of the 5V-output circuit becomes $H_{5V}(s) = \frac{5}{5} = 1$ and the 12V-output sensor gain becomes $H_{12V}(s) = \frac{5}{12}$. The gain of the pulse width modulator is $G_{PWM}(s) = \frac{1}{V_m} = \frac{1}{5}$, where $V_m$ is the peak value of the sawtooth carrier.

Loop gain $T(s)$ of the any output circuit of the forward converter is,

$$T(s) = H(s).G_c(s).G_{vd}(s).G_{PWM}(s) \tag{B.1}$$

$G_c(s)$ should be designed such that, converter must be stable for its entire operation range and provide good transient response. Choosing cross-over frequency about one twentieth of the switching frequency and remaining at least 45 degree of phase margin near crossover frequency for the worst case operating point provides enough control performance [16]. In this work controllers for each output circuit are designed in such a way that desired performance criteria are provided for the case of input voltage and output currents are at their rated values, that is $V_g$ = 42V, $I_{o1}$ = 10A for 5V-output and $I_{o2}$ = 4A for 12V-output. The designed controller for this operating point is also checked for the case of minimum input voltage, $V_g$ = 32V, while output currents are at their rated values in order to guarantee the stable and high performance operation. Minimum input voltage and maximum output current operation is the worst case condition in terms of voltage regulation.

### B.1 Controller Design for 5V-Output:

Control-to-output transfer function for the 5V-output is given by the help of equation (3.26) (here, output number k=1) which is given below,

$$G_{vd_1}(s) = \frac{v_{o1}(s)}{d_1(s)} = n_1 V_g \frac{1}{s^2 L_{o1} C_{o1} + s\frac{L_{o1}}{R_{o1}} + 1} \tag{B.2}$$

where $n_1 = \frac{6}{11}$ is the turns ratio of the transformer from primary to 5V-output winding. $L_{01} = 0.1mH$ and $C_{01} = 3500\mu F$. $R_{01} = 0.5\Omega$ which gives 10A output current for 5V-output. Putting those parameters into the equation (B.2), control-to-output transfer function for 5V-output circuit becomes

$$G_{vd_1}(s) = \frac{22.9}{s^2 0{,}35.10^{-6} + s0{,}02857 + 1} \tag{B.3}$$

Loop gain $T_1(s)$ of the 5V-output circuit of the forward converter is given as

$$T_1(s) = H_{5V}(s).G_{c1}(s).G_{vd1}(s).G_{PWM}(s)$$
$$T_1(s) = 1 \times G_{c1}(s). \times \frac{22.9}{s^2 0{,}35.10^{-6} + s0{,}02857 + 1} \times \frac{1}{5} \tag{B.4a}$$

For uncompensated system $G_{c1}(s)$=1 and $T_1(s)$ becomes

$$T_{1u}(s) = \frac{4{,}58}{s^2 0{,}35.10^{-6} + s0{,}02857 + 1} \tag{B.4b}$$

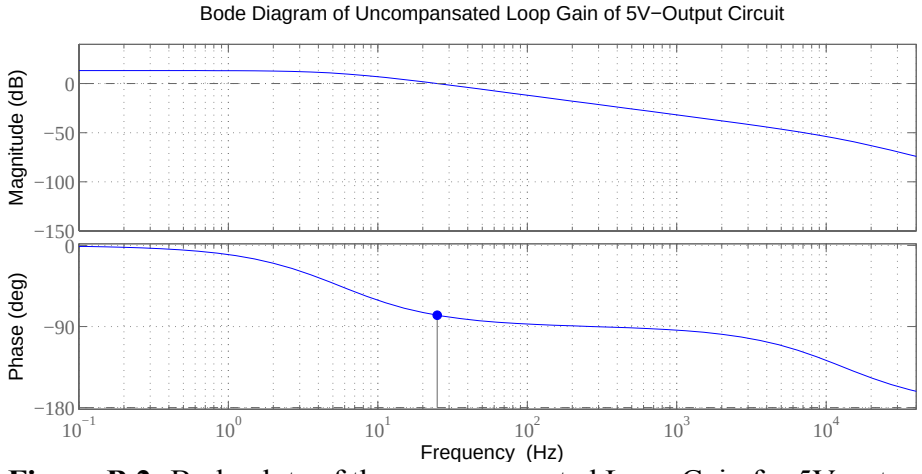


**Figure B.2:** Bode plots of the uncompensated Loop Gain for 5V-output.

Figure B.2 shows the Bode diagram of the uncompensated $T_{1u}(s)$. Cross-over frequency of $T_{1u}(s)$ is $f_c$ = 25Hz and phase margin $PM$ = 102 degree at this frequency. $T_{1u}(s)$ is stable; however bandwidth is not enough for fast transient response.

In this work $G_{c1}(s)$ is designed such that $T_{1u}(s)$ has a bandwidth of $f_o$ = 1kHz and phase margin of $PM$ = 75 degree for rated operating conditions such that $V_g$ = 42V, and $I_{o1}$ = 10A. At the operating point $V_g$ = 32V, $I_{o1}$ = 10A, the controller provides

bandwidth of $f_o$ = 760Hz and phase margin of $PM$ = 79 degree. Therefore, the controller for 5V-output $G_{c1}(s)$ is given below:

$$G_{c1}(s) = \frac{40}{1 + 2{,}9.10^{-5} s} \tag{B.5}$$

Figure B.3 shows the compensated loop gain for 5V-output.

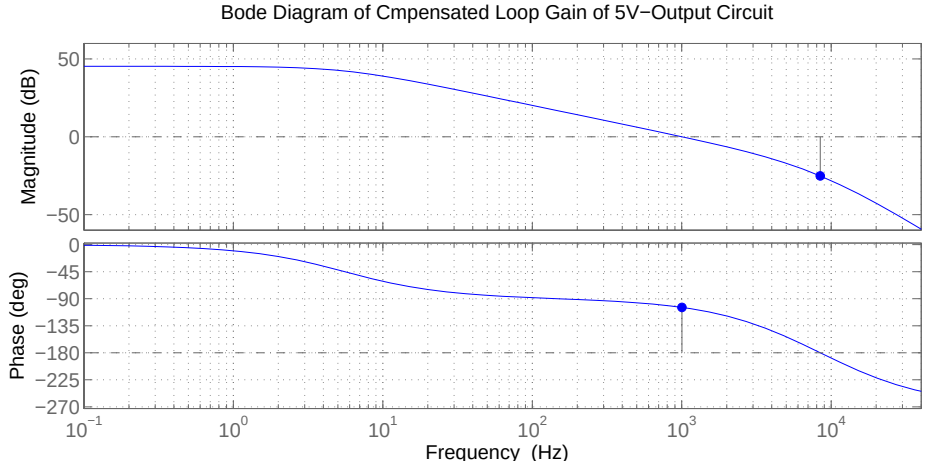


**Figure B.3:** Bode plots of the compensated Loop Gain for 5V-output

### B.2 Controller Design for 12V-Output:

Control-to-output transfer function for the 12V-output is given by the help of equation (3.26) (here, output number k=2) which is given below,

$$G_{vd_2}(s) = \frac{v_{o2}(s)}{d_2(s)} = n_2 V_g \frac{1}{s^2 L_{o2} C_{o2} + s\frac{L_{o2}}{R_{o2}} + 1} \tag{B.6}$$

where $n_2 = \frac{13}{11}$ is the turns ratio of the transformer from primary to 12V-output winding. $L_{02} = 0.2mH$ and $C_{01} = 2470\mu F$. $R_{02} = 3\Omega$ which gives 4A output current for 12V-output. Putting those parameters into the equation (B.6), control-to-output transfer function for 12V-output circuit becomes

$$G_{vd_2}(s) = \frac{49{,}636}{s^2 0{,}4941.10^{-6} + s0{,}08 + 1} \tag{B.7}$$

Loop gain $T_2(s)$ of the 12V-output circuit of the forward converter is given as

$$T_2(s) = H_{12V}(s).G_{c2}(s).G_{vd2}(s).G_{PWM}(s)$$

$$T_2(s) = 1 \times G_{c2}(s). \times \frac{4.136}{s^2 0{,}4941.10^{-6} + s0{,}08 + 1} \times \frac{1}{5} \tag{B.8a}$$

For uncompensated system $G_{c2}(s)$=1 and $T_2(s)$ becomes

$$T_{2u}(s) = \frac{4{,}136}{s^2\, 0{,}4941.10^{-6} + s0{,}08 + 1} \tag{B.8b}$$

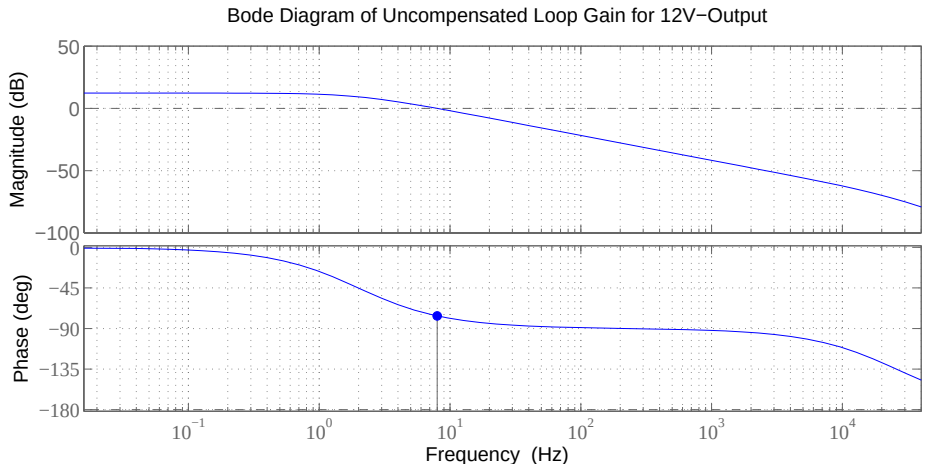


**Figure B.4:** Bode plots of the uncompensated Loop Gain for 5V-output.

Figure B.4 shows the Bode diagram of the uncompensated $T_{2u}(s)$. Cross-over frequency of $T_{2u}(s)$ is $f_c$ = 8Hz and phase margin $PM$ = 104 degree at this frequency. $T_{2u}(s)$ is stable; however bandwidth is not enough for fast transient response.

In this work $G_{c2}(s)$ is designed such that $T_{2u}(s)$ has a bandwidth of $f_o$ = 400Hz and phase margin of $PM$ = 75 degree for rated operating conditions such that $V_g$ = 42V, and $I_{o2}$ = 4A. At the operating point $V_g$ = 32V, $I_{o2}$ = 4A, the controller provides bandwidth of $f_o$ = 307Hz and phase margin of $PM$ = 79 degree. Therefore, the controller for 12V-output $G_{c2}(s)$ is given below:

$$G_{c1}(s) = \frac{50}{1 + 0{,}0001s} \tag{B.9}$$

Figure B.5 shows the compensated loop gain for 12V-output.

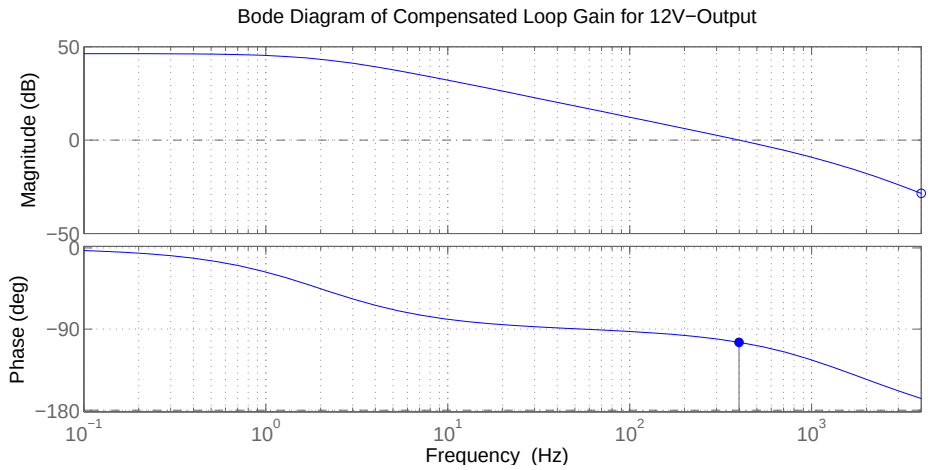


**Figure B.5:** Bode plots of the compensated Loop Gain for 12V-output.

## BIOGRAPHY

Şükrü ERTİKE was born in 1979 in Sivas, Turkey. He graduated from Ankara Çankaya High School in 1997. He has two B.Sc. degree from Istanbul Technical University; one is Electrical Engineering (1999-2004) and the other one is Electronics and Communication Engineering (1999-2004). He studied as R&D engineer in a company between the years 2004-2005. He is a Research Assistant in ITU Electrical Engineering Department since December 2005.